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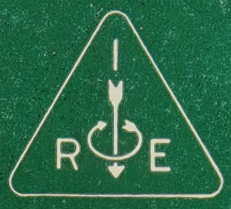

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Improvements to Current Switching*

F. K. BUELOW†, MEMBER, IRE

Summary—Diode switching circuits have been used in conjunction with emitter followers and current switching circuits to solve a new set of system building blocks. These blocks exhibit typical delays under five millimicroseconds. Diodes cost less and are physically smaller than transistors; therefore, this new system is cheaper and faster than an all-current switching system and permits at least a fivefold increase in packaging density.

Introduction

THIS PAPER describes a circuit technique used to obtain logic blocks with delays under five millimicroseconds. A wide range of transistor and diode types were used. The transistors can be generally characterized as 200-mw transistors with a gain-bandwidth product greater than 400 megacycles and emitter-base breakdown voltages of over 3.5 volts. The diodes have recovery times which are typically less than 3 mμsec when switched from 3 ma forward to 6 volts through 2 kilohms. These components represent some of the highest speed transistors and diodes that are commercially available and were used in an effort to obtain high switching speeds. However, the basic circuit technique is applicable to lower speed, lower cost devices.

Basic Circuit

The basic circuit concept consists of current-switching (hereafter referred to as CS) circuits[1] supplemented by diode-switching circuits and emitter followers (EF's). (See Fig. 1 for the combined circuit.) Current-switching circuits and emitter followers have the inherent high-speed advantage of operating out of saturation. CS circuits also have good sensitivity to small signal swings, well-defined output signal levels, fast rise and fall times, and both normal and inverted output signals. Unfortunately, the standard CS logic block[1] requires an additional transistor for each logical input. In addition to being expensive, the extra transistors slow up switching times because they add capacitance at the common emitter and collector nodes. An alternative to an all-CS system is to replace some of the CS blocks by diode blocks. If diodes are used at the input, then the output of the CS block must be made capable of driving diodes. This requires a high-current driver such as an emitter follower.

If we build such a system of diode-CS-EF circuits, the delay across the emitter followers and diodes is typically under 2 mμsec, while, because of the increased base drive, the CS block switches 2 or 3 mμsec faster than in an all-CS system. Since diodes and CS circuits represent two levels of logic, we have an effective reduction in logical delay of approximately 50 per cent. In this case, either diode AND's or diode OR's could be used at each input to the CS circuit which acts as an OR, level setter, and inverter. However, any logical expression can be reduced, by well-known means, to a minimum sum form. Circuit implementation of this form requires AND's feeding one (and only one) OR. To be logically complete, the option of an inverted output must be available. This leads directly to the circuit shown in Fig. 2.

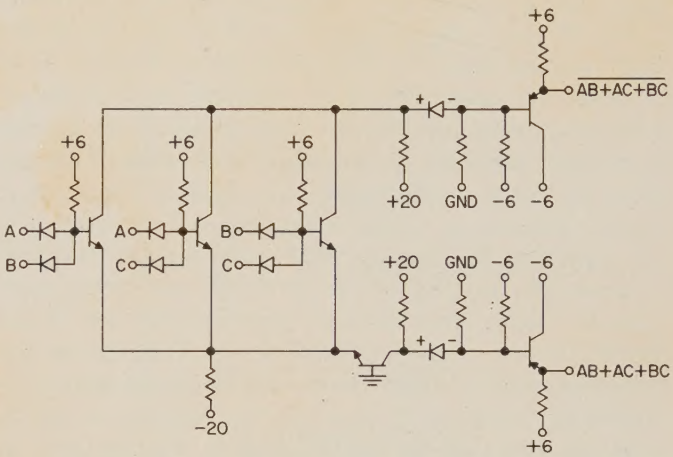

Fig. 1—Diode extension to current switching.

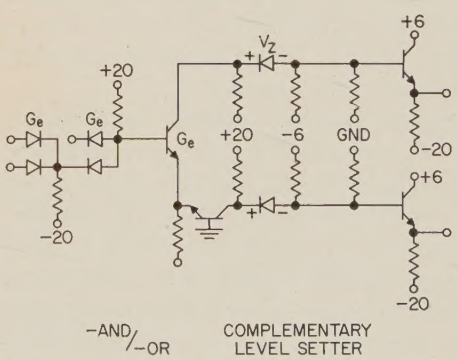

Fig. 2—Basic logic block. This block can readily implement the minimum sum form of any function.

Designing for one, and only one, OR directly on the output of the AND means that EF's are needed only for driving AND's; therefore, only one type of transistor is required. If *n-p-n*'s are chosen, it is convenient to let a negative voltage level represent a logical "one."

* Received by the PGEC, April 1, 1960. The work reported here was supported by the AF Cambridge Res. Ctr. under Contract No. AF19 (604)-4152.

† Product Dev. Lab., Data Systems Div., IBM Corp., Poughkeepsie, N. Y.

[1] H. S. Yourke, "Millimicrosecond transistor current switching circuits," IRE TRANS. ON CIRCUIT THEORY, vol. CT-4, pp. 236–240; September, 1957.

The problem of different dc levels at the input and output of the CS is eliminated by the use of a zener diode as a class A dc translator.

If signal level and rise time are reasonably well preserved at the output of a diode OR, level setting may not be required. Then it becomes possible to do without the CS (provided inversion is not also required), and simply couple diode stages with EF's as shown in Fig. 3. (The reason for the core in the emitter circuit is explained below.) If a silicon diode is used as an OR, this circuit can be balanced to show no nominal dc shift from input to output.

Design Considerations

The emitter-base breakdown voltage of the CS transistors sets a limit on the maximum allowable signal swing. With such a signal swing, the maximum number of diode-EF stages between CS blocks is limited by signal attenuation and dc shift. If all components are at their worst-case tolerances, the signal shift is so large that it is difficult to design for two stages of diode-EF's. However, the probability of all transistors, diodes, and resistors being at their worst-case tolerance seems remote. We have, therefore, resorted to a synthetic sampling technique (Monte Carlo method[2]) to develop a realistic estimate of the possible dc shift. This was done by using an IBM-704 to randomly choose component parameter values within given limits and with any specified distribution. The computer was then used to solve an equation for the particular performance parameter under consideration, once for each set of randomly chosen component parameters. This process was repeated, usually 10,000 times, and the results were automatically tabulated to give the distribution of the desired performance parameter (Fig. 4). Statistically, we have found that a reasonable number of stages based on this method is approximately twice as many as would be indicated by a worst-case design philosophy. If the unlikely combination of worst-case components does occur, it will be found in testing assembled circuits before inclusion in a machine.

Long chains of emitter followers and diodes, although permitted in a dc analysis, have an unhappy tendency to oscillate. Figs. 5 and 6 show the more common modes of oscillation. With 500-Mc mesa transistors, 3 or 4 $\mu\mu$f of stray capacitance from emitter to base [Fig. 5(a)] will yield oscillations in the 50 to 100-Mc range. Very small values of stray inductance at the collector [Fig. 5(b)] will cause oscillations in the 250 to 500-Mc range. Careful packaging can eliminate these two feedback modes, but two other modes are still possible. An examination of the transfer function of an emitter follower will show that ringing is almost inevitable with a good voltage drive at the base. Fortunately, our transient drive is more closely approximated by a constant current source. Finally, if the input impedance is measured or calculated as a function of frequency [Fig. 6(b)] it is found to be a negative resistance and capacitive reactance over a wide frequency spectrum. If sufficient inductance is present at the base, large oscillations can occur (10 volts peak-to-peak with ± 6

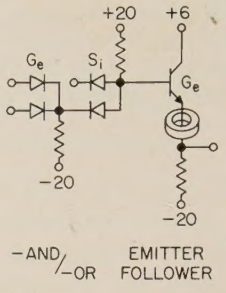

Fig. 3—Emitter follower coupled with diode AND/OR stage.

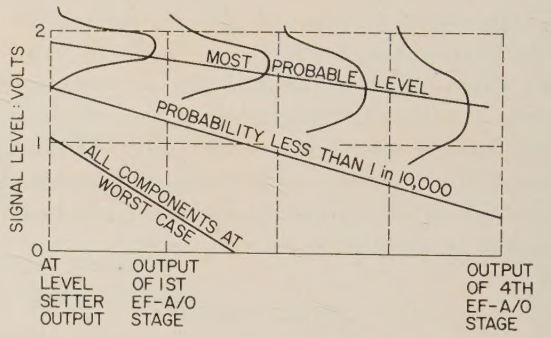

Fig. 4—Statistical analysis of signal levels. A synthetic sampling technique (Monte Carlo method) was used to develop a realistic estimate of the probable failure rate.

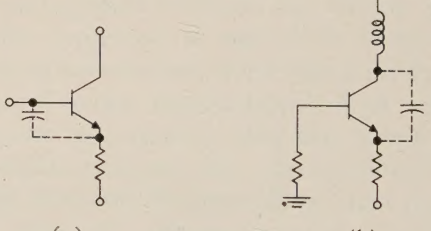

Fig. 5—Oscillation modes in emitter followers due to feedback through stray capacitance and inductance.

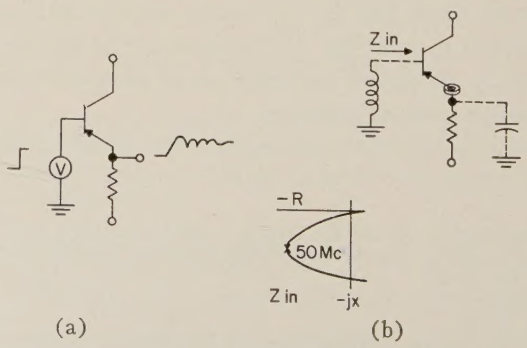

Fig. 6—Oscillation modes in emitter followers due to low base impedance or stray inductance at the base.

[2] L. Hellerman, "Monte Carlo Analysis and Design Programs," IBM Corp., New York, N. Y., Tech. Note No. TN00. 11000. 354; April, 1959.

lt supplies). Fortunately, with the small values of ray inductance usually encountered, matching of ductance to base capacitance occurs only at very high equencies where the negative input resistance is small. this small negative resistance proves troublesome, rious means of compensation can be used. More care- l wiring, additional resistance in the base or emitter, feedback from collector to base are all effective for abilization, but the most generally useful in our appli- tion is a ferrite core at the emitter. This acts as a ssy inductance which will help compensate for stray pacitance and yet does not affect the dc levels. Fer- te cores and careful wiring will permit chain lengths four to six diode-EF stages between CS circuits.

Circuit Delay

If we attribute no logical usefulness to the CS circuit, s would be the case when it is used only for level set- ng, then the average delay of a logic block in any ain of logic is reduced by limiting the use of CS cir- its. Clearly, the longer a chain of diode-EF stages etween CS circuits, the smaller the average delay. The act measurement of delay is somewhat difficult. The mpedance level is high enough at most points to be ffected by an oscilloscope probe. At low-impedance oints, such as CS outputs, the rise time is generally ster than the minimum rise time of available oscillo- opes. Somewhat arbitrarily, we have elected to take elay measurements at the 50 per cent point of transi- ons at CS outputs, and to average the delay for the umber of logic blocks between CS circuits. A typical elay measurement and typical waveforms are shown Figs. 7 and 8. In this case, we have two-input AND's feeding two-input OR's with a fan-out of 5 from EF's. Inputs to AND's and OR's are biased to simulate worst-case diode recovery at all points. Fig. 8 shows the deterioration in fall time under these conditions. The apparent total lack of delay across the CS is due to loading of the input waveform by the oscilloscope probe. For this typical case, we have a total delay of approximately 20 mμsec across 6 diode-EF stages and a CS circuit representing, in all, 12 levels of logic, or an average delay per logic block of 1.7 mμsec. Further variations in component tolerances, power supplies, additional wiring capacitance, and chain lengths will yield a possible skew between best and worst cases as shown in Figs. 9 and 10. A reduction in fan-out will reduce both best- and worst-case delays. These circuit delays are very strongly influenced by packaging. Wire lengths are very important because of the loading effects of stray capacitance as well as the basic limit of 1 mμsec per foot propa-

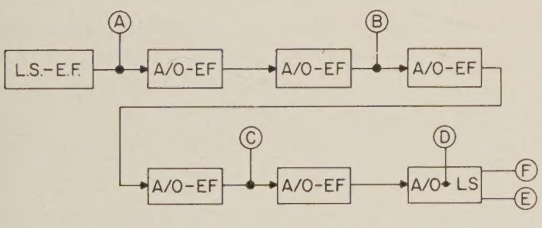

Fig. 7—Typical chain for delay measurements.

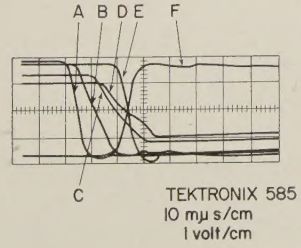

Fig. 8—Typical waveforms with worst-case diode recovery

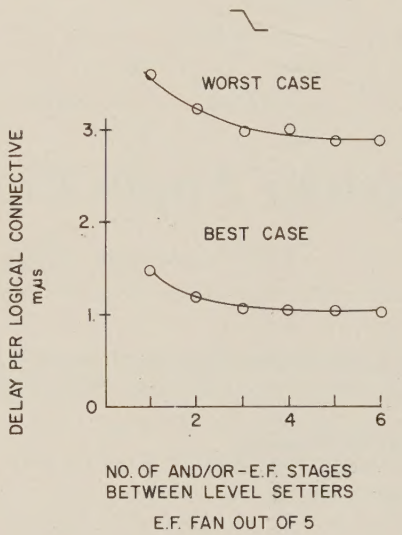

Fig. 9—Best-case and worst-case propagation delay on the negative-going transition.

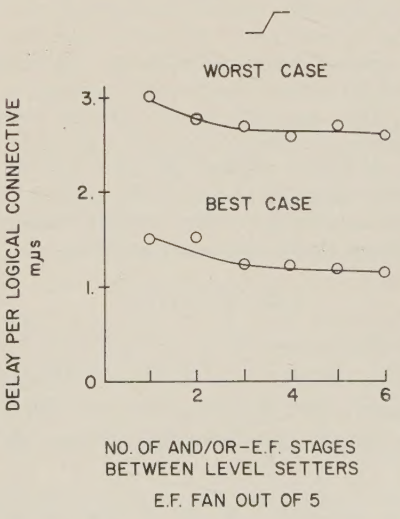

Fig. 10—Best-case and worst-case propagation delay on the positive-going transition.

gation velocity. Compact packaging and the associated short wire lengths become a goal simply to obtain high-speed operation.

The diode circuits presented here lend themselves to very simple, compact packaging. An examination of the full adder shown in Fig. 11 shows how easily a three-dimensional array is achieved. The diodes shown can be packaged readily in a 1-inch × 1-inch × ½-inch space. When intermixed on a printed-wiring card with transistors and other components, the net effect is a five to tenfold increase in circuit density over an all-CS system. Any further increase in density would increase the power density to the point where conventional air cooling techniques are not adequate. These circuits therefore not only offer a high speed potential, but they do so at a lower cost than all-transistor circuits. Further, because of the ease of packaging, they can be easily adapted to existing machine systems.

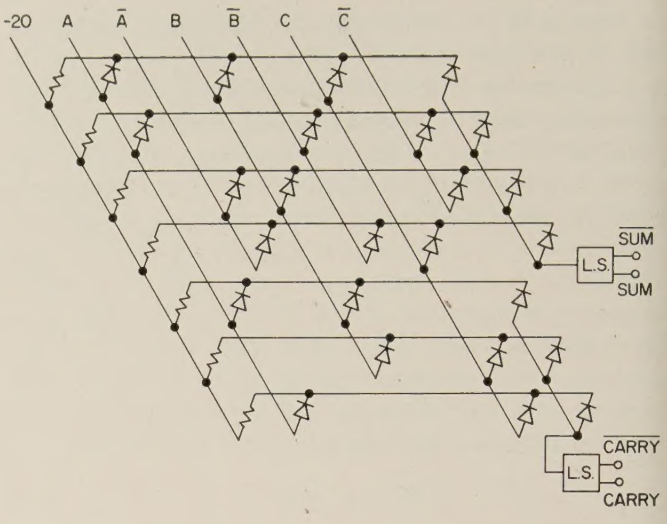

Fig. 11—Full adder with diodes arranged in a three-dimensional matrix.

System Application of Hybrid Logic Circuitry*

J. T. LYNCH†, MEMBER, IRE, AND J. J. KAREW†, MEMBER, IRE

Summary—A comparative performance rating of circuit techniques for performing logical functions in digital systems may be based upon:

1) Reliability and simplicity
2) Input and output capabilities
3) Propagation time
4) Cost.

The "Hybrid Transistor Diode Logic" (HTDL) circuit technique employs either diodes or emitter follower transistors as gates and buffers, to maximize the circuit performance rating. The HTDL technique thus combines the advantages of lumped and distributed gain circuits. The cascading of diodes and emitter followers in logical gate matrices can be analyzed as the transmission of binary signals through a video system of a given bandwidth. The HTDL technique optimizes the use of the transistor through nonsaturating, low-impedance circuitry. This optimum use of 200–500 megacycle gain-bandwidth transistors is primarily limited by present-day packaging techniques and their inductive and capacitive loading effects upon the circuits. The development of macromodule packaging techniques, using 200–500 mc transistors, in HTDL circuitry, would permit system speeds (synchronous clock rates) to exceed 50 Mc.

Introduction

THE performance rating of digital logical elements, normally composed of gates (AND-OR), toggles (flip-flops), and buffers (logic amplifiers), can be evaluated in terms of a functional figure of merit [1]. This figure of merit can be based upon:

1) Reliability and simplicity of the logical elements,
2) Permitted number of inputs and outputs (fan-in and fan-out) per logical element,
3) Propagation time per logical element,
4) Cost per logical element, including maintenance cost.

There exist many circuit techniques [2]–[7] for performing logical functions, and they can be generally classified into two principal operational modes:

1) Lumped-gain system (passive gates, such as diodes, with buffers distributed throughout the logic network);
2) Distributed-gain system (active gates, such as transistors, which perform the dual functions of gating and buffering).

Most of the techniques incorporate either of these two modes but rarely combine the two in any one system.

The study of a typical logic flow chain, such as in the arithmetic or control section of a synchronous digital computer, indicates that the logic signal normally has a large divergence (fan-out) requirement at the output of a storage element (flip-flop). This fact dictates that buffers are required to supply the necessary power to the large number of gates to be driven. The output requirement of the chain converges to one as the logic signal

* Received by the PGEC, March 11, 1960; revised manuscript received, August 22, 1960.

† Great Valley Lab., Burroughs Corp., Paoli, Pa.

ropagates to the input of the second storage element lip-flop). This fact indicates that passive gates can be sed at the end of the logic chain, since the output re-uirements diminish to driving only the single input to a ip-flop. Therefore, a crossover or combinations of the istributed-gain system to the lumped-gain system ould be desired, at certain areas in the chain, to maxi-ize the system flexibility and efficiency. A circuit tech-ique which essentially combines the distributed and mped-gain modes in any desired combination that is equired by the system would be very desirable.

Hybrid Transistor-Diode Logic

The hybrid transistor-diode logic[1] matrix, shown in ig. 1, can best be explained by its function. Assuming he logic polarity[2] to be negative, we find the first net-ork to be a multiple input AND gate which can con-st of either *n-p-n* transistors or ordinary diodes. For he requirement of a fan-out of only one at output 1, he gate would consist of diodes. (The collector-base iodes would vanish; the connection is opened at the otted line, to indicate the need for only diodes.) For he requirement of a large fan-out (2–12 gates) at out-ut 1, the gate would consist of *n-p-n* transistors.

The current drain through the node resistor (R_1 in ig. 1) can be held to a minimum, for the node is acti-ated by the emitter-follower transistor, which performs he dual function of gate and buffer. The second logic etwork is a multiple input OR gate that can consist of ither *p-n-p* transistors or ordinary diodes. Once again, or the requirement of a fan-out of only one at output 2, he gate would consist of diodes. (The collector-base iodes would vanish; the connection is opened at the otted line, to indicate the need for only diodes.) For the equirement of a large fan-out (2–12 gates) at output 2, he gate would consist of *p-n-p* transistors. The tran-istor gate network would have the normal logic signal utput at output 3. If diodes were normally used for the ND-OR function, the *n-p-n* emitter-follower, which is ascaded with the *p-n-p* emitter-follower, could act as he logic buffer. This lumped buffer would provide a arge fan-out (2–12 gates) capability at output 4.

The diodes connected between input and output for ach emitter-follower (CR-1 and CR-2 for Q_1 and Q_2, espectively) permit rapid negative and positive transi-ion of the logic signal at output 4 by coupling the out-ut load closely to both polarity amplifiers. This tech-ique produces an effective push-pull buffer, with Q_1 ulling up and Q_2 pulling down.

The amplitude of the logic voltage, less than V_e, llows for minimum logical gate delay, since the emitter-ollowers are employed in a nonsaturating mode. The

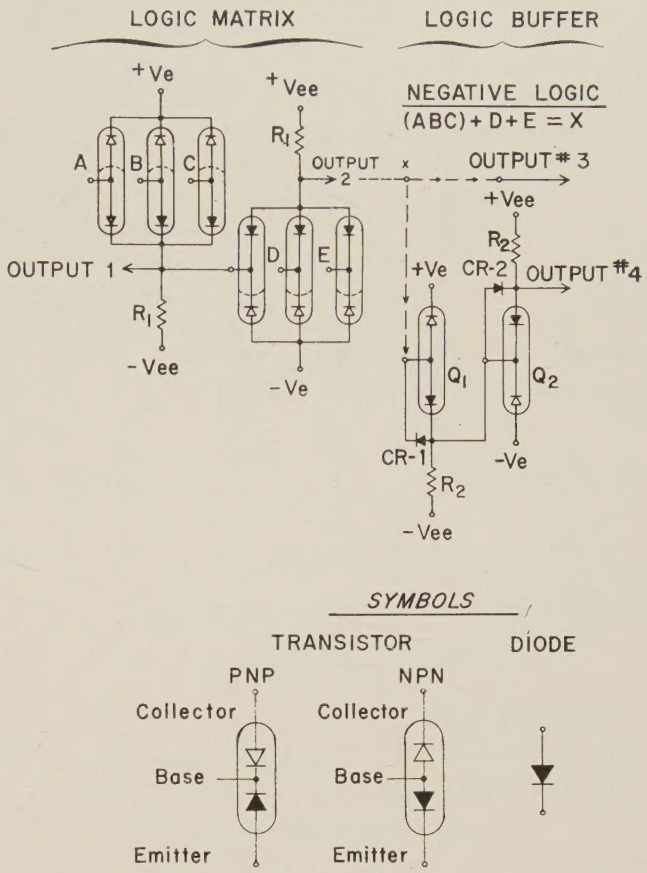

Fig. 1—Hybrid transistor diode logic network.

absence of voltage amplification is not a system hindrance, because the alternation of *p-n-p* and *n-p-n* transistors or "AND" diodes and "OR" diodes provides for minimum level shifting of the logic signal. The use of the complementary transistors permits the implementation of a double-ended system ($+V_e$ to $-V_e$) and thereby operates with complementary-symmetry storage elements [8]. A typical logic matrix for a practical system is shown in Fig. 2. Fig. 2 shows that the number of components per gate is $n+1$, where n is the number of inputs.

It is interesting to note here the evolution of solid-state gate circuitry; Fig. 3 is a record of the various types of gate circuitry, their delay per stage as experienced in a practical system, and the approximate date that the particular circuitry appeared in a system. The figure also gives a comparative circuit cost per three-input gate for the various magnitudes of delays listed. It is seen that the 100-nanosecond gate can be implemented for one seventh of the cost and with the same number of components with hybrid logic as with the DCTL approach. Another comparison is that, for approximately three times the price, the hybrid circuitry provides a 50 to 1 decrease in delay per stage.

General Design Considerations

In the hybrid technique, the operation of the transistor as an emitter-follower, in its linear region, per-

[1] The technique of using both diodes and transistors is not new. he technique was first disclosed by Burroughs at an IRE 4.1 com-ittee meeting at Denver in 1958. It is also known that the CG-24 mputer, built at the M.I.T. Lincoln Laboratory, Lexington, Mass., es much the same approach.

[2] The logical "1" defined as the more negative state of the two gnal levels.

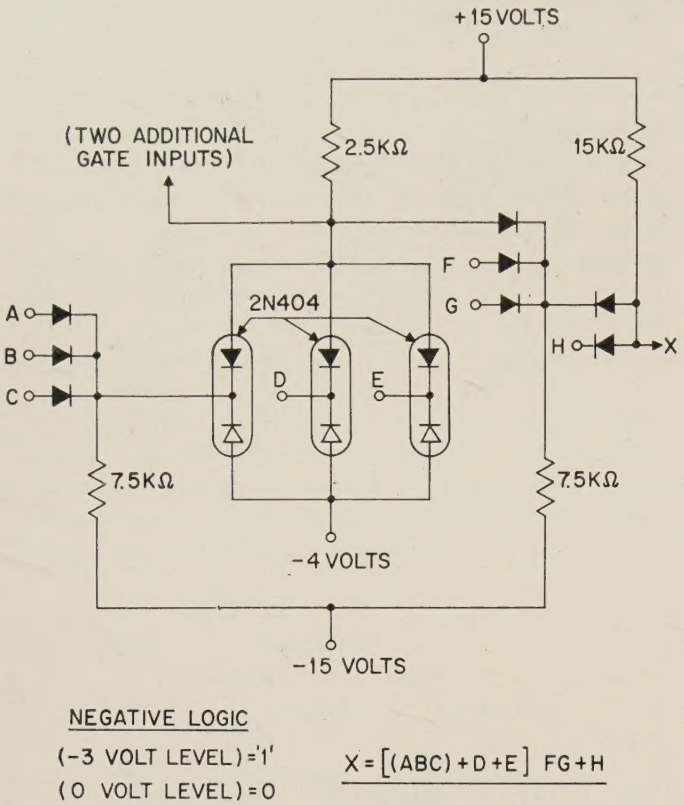

Fig. 2—Typical gate matrix.

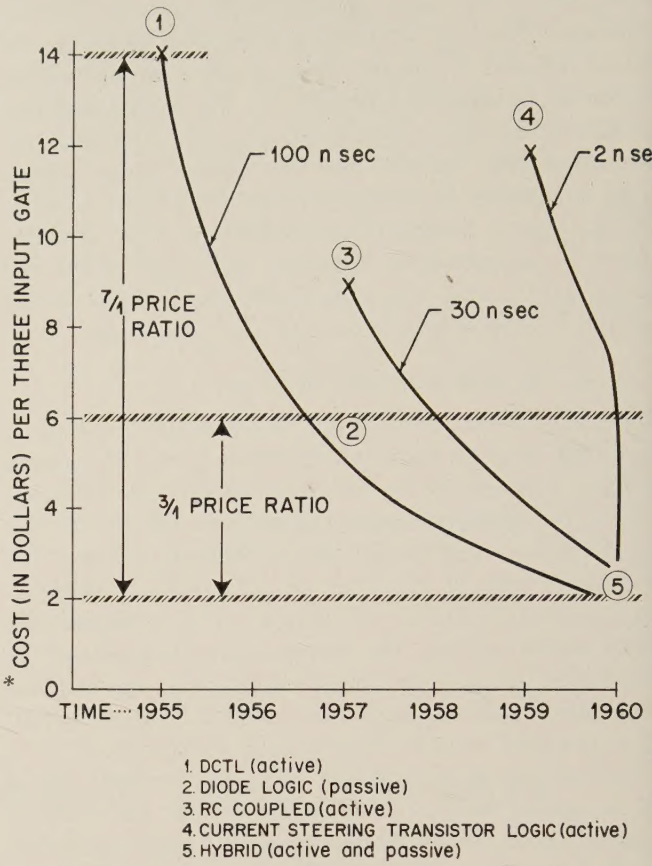

Fig. 3—Evolution of gate circuitry.

mits the use of cascaded video amplifier analysis to be applied. In such a system, the propagation of a pulse with a specified transition time is dependent upon the composite frequency bandwidth of the system. The composite bandwidth is dependent upon the active device (transistor) and the passive-circuit (RC) bandwidth. For a given transistor gain-bandwidth figure of merit, the composite system bandwidth can be maximized by increasing the power consumption of the system (minimization of the circuit resistance). A simplified expression for the transition time can be given as [9]

$$t_c = A(T_a + T_p) \ln \frac{1}{1 - 0.9\left[\frac{V_0}{V_i}\cdot\frac{1}{A}\right]}, \qquad (1)$$

where

t_c = circuit transition time (0 to 90%),
T_a = time constant of transistor ($1/\omega_{c\alpha}$),
T_p = passive circuit time constant = RC,
V_0 = output voltage swing,
V_i = input voltage swing,
A = transistor amplification factor (limits between α and $\alpha/(1-\alpha)$).

As seen from the expression for transition time, the circuit can be limited by the passive or the active time constants.

If we were to plot the dependence characteristics of transition or propagation time normalized with respect to the transistor time constant (T_a), we would obtain a curve as shown in Fig. 4. This figure essentially shows that the plot of circuit transition or propagation time as the magnitude of the passive time constant (resistor circuit capacitance product, neglecting any inductive effects) is varied by means of increasing or decreasing the magnitude of the gate current.

In synchronous digital systems, the allowable propagation time for a logic gate, for a given clock repetition rate, is limited by the propagation time through the storage element (flip-flop) and the number of logic gates required in the logic matrix chain. This can be defined in time as

$$t = t_1 + nt_2, \qquad (2)$$

where

t = time between clock pulses,
t_1 = propagation time through flip-flop circuit,
t_2 = propagation time through gate circuit,
n = number of gates required in chain.

The propagation of a pulse with a specified transition period can be maintained if the frequency bandwidth of the system equals or exceeds the relationship [10]:

$$BW(n) = \frac{0.35}{t_c}, \qquad (3)$$

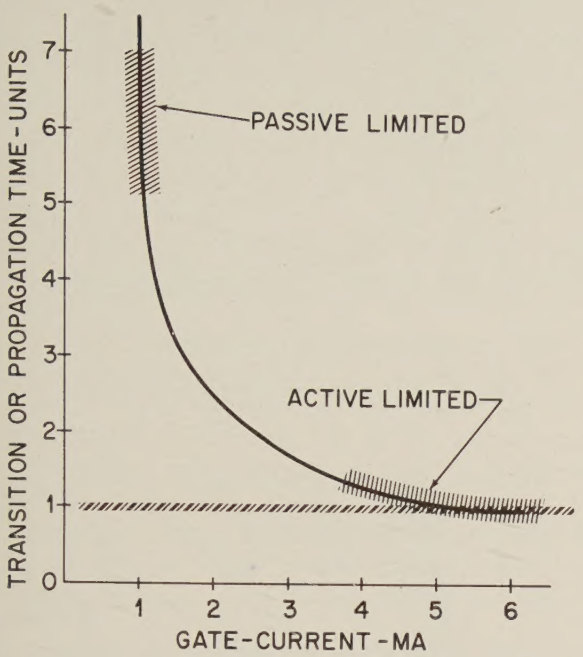

Fig. 4—Passive-active propagation time trade-off.

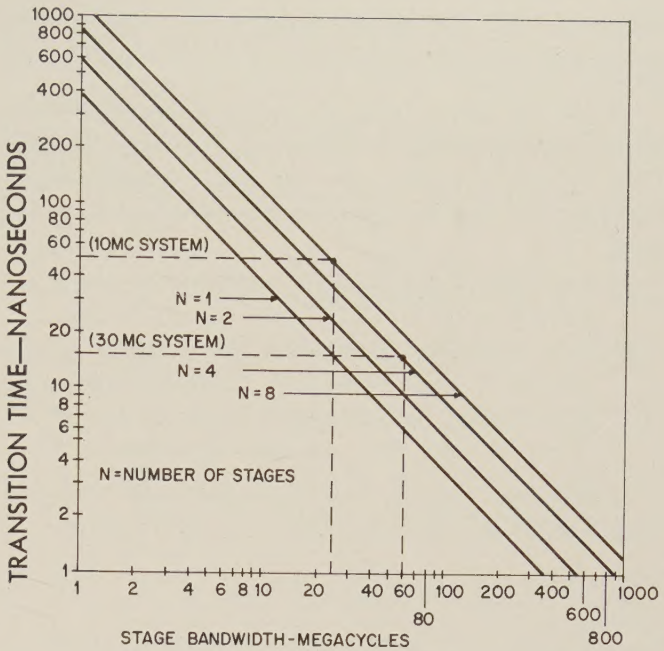

Fig. 5—Transition time bandwidth chart.

where

BW(n) = frequency bandwidth of n stages,

t_c = transition time of pulse being propagated.

The bandwidth of a single circuit in a chain of (n) homogeneous video stages must have a bandwidth as indicated by [11]:

$$\mathrm{BW}(1) = \frac{\mathrm{BW}(n)}{[2^{1/n} - 1]^{1/2}} \tag{4}$$

by combining (3) and (4)

$$\mathrm{BW}(1) = \frac{0.35}{t_c[2^{1/n} - 1]^{1/2}} \cdot \tag{5}$$

A graph (Fig. 5) for determining the bandwidth per stage $n = 1, 2, 4, 8$ for the propagation of a defined transition period pulse can be applied to aid designing the system.

Example

For a 100-nanosecond (10-Mc) clock rate, the required number of logic stages in a chain is eight. The maximum transition time pulse that can be propagated without loss of amplitude is equal to one half the clock rate, or 50 nanoseconds. From Fig. 5, a single stage, in a cascaded chain of eight stages, must have a composite bandwidth of at least 25 Mc to be able to propagate a pulse with 50 nanoseconds transition time.

System Consideration

The design of the individual circuit is only the first step to the successful utilization of the circuit in the system.

Some of the system aspects which must be considered when specifying a logical building block employing a given circuit are:

1) Lead inductance and line capacity,
2) Fan-in, fan-out requirements,
3) Packaging concept,
4) Machine organization.

The relative importance of these items is primarily a function of the speed of the system. For a low-speed machine, the individual circuits can easily be designed to incorporate the system requirements, but for a high-speed machine, an electronic engineering effort must be carried into the machine-fabrication stage.

The point that the above items play in a high-speed machine can be illustrated by discussing the problems and the solutions associated with three high-speed machines that have been or are being constructed. For purpose of discussion the three machines can be described as:

Machine	*Synchronous Repetition Rate*	*Component Count (approx.)*	*State of Construction*
A	7 Mc	30,000	completed
B	30 Mc	5,000	completed
C	10 Mc	1,000,000	under fabrication

Machine A was a test vehicle designed to investigate the problems associated with high-speed systems. Machine C is the outgrowth of the project. Machine B was another test vehicle concerned with the problem in the 20–50 Mc region.

The first step in all these systems is the initial circuit breadboard. At this point, the compromise must be made between the theoretical limits in machine speed and practical considerations. It is possible to mechanize small systems with repetition rates in excess of 50 Mc, where the individual gate delays are less than a nanosecond. Such a machine must be bought at a high price,

however, and the price to be paid includes large power consumption and restricted fan-in fan-out capability.

The 30-Mc system (Machine B) is an attempt to convert a large portion of the theoretically attainable speed into a working system. The two major conditions that the logicians and the packaging people had to satisfy were:

a) The differential fan-out capability of a gate was limited to two.
b) The cumulative number of feet of hook-up wire could not exceed three feet. (The signal delay per foot of wire, including two inches of printed circuitry, is about four millimicroseconds.)

In order to describe a system adequately, (2) (discussed in the previous section) must be rewritten:

$$t = t_1 + nt_2 + t_3 \tag{6}$$

when t, t_1, n, and t_2 are as defined, and t_3 is the delay due to cumulative wire length between storage elements. For the 30-Mc machine, $t = 33$ nanoseconds, $t_1 = 12$ nanoseconds, $n = 8$, $t_2 = 1$ nanosecond, and $t_3 = 10$–12 nanoseconds. Note that a full one-third of the delay is due to the packaging concept employed. Machine C, because of the 1,000,000 components required to mechanize the system, pays a much more severe packaging penalty. In this system, even if the logical circuits introduced zero delay, machine speed would be limited to 20 Mc.

Packaging density, when one contemplates a high-speed machine, has thus become at least as important as the circuitry. Packaging is important not only because it contributes heavily to logical delay, but also because it directly affects the back-plane layout. In fact, packaging is often the limit in the fan-out capability of a driving source. For the 10-Mc system the charts shown in Figs. 6 and 7 were generated as an aid to machine layout.

Fig. 6 is an inductive noise determination chart. The maximum tolerable noise voltage was limited to 10 per cent of the signal voltage or 0.3 volts, and was calculated on the basis of $v_{noise} = L(\Delta I/\Delta T)$ for a specified wire inductance per unit length. The chart in Fig. 6 must be satisfied in order to keep the inductive noise level to less than 0.3 volt, or 10 per cent of the logical signal level. To satisfy this condition for a given transition time associated with the logical signal, a maximum current-length product of 15 milliampere feet (ma-ft) of open hook-up wire should not be exceeded. This means that a lead for a single AND gate (approximately 2.3 ma) would be limited to a length of six feet if the limit of inductive noise generated were the only consideration. If there were four gates located three feet from the source of drive, a single line could not be used for transmission because of the induction noise generated ($4 \times 2.3 \times 3 > 15$).

The limit in branching many less heavily loaded lines is determined by Fig. 7, which was generated on the

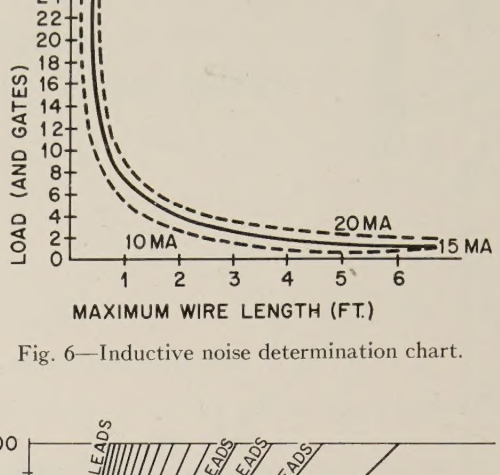

Fig. 6—Inductive noise determination chart.

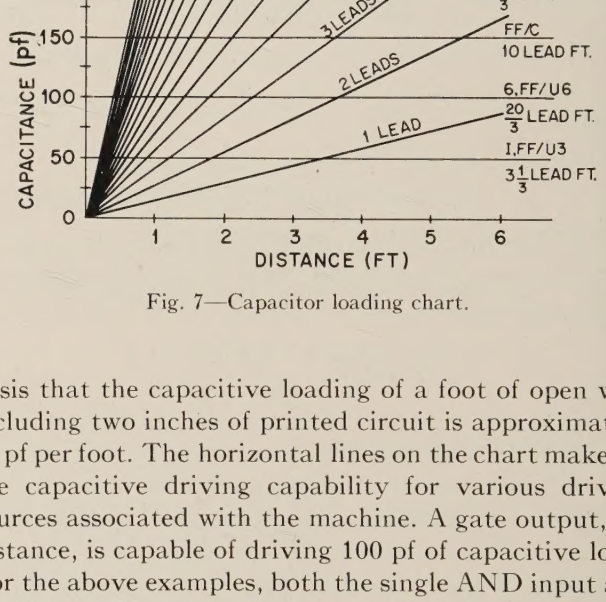

Fig. 7—Capacitor loading chart.

basis that the capacitive loading of a foot of open wire including two inches of printed circuit is approximately 15 pf per foot. The horizontal lines on the chart make up the capacitive driving capability for various driving sources associated with the machine. A gate output, for instance, is capable of driving 100 pf of capacitive load. For the above examples, both the single AND input and the four AND inputs being fed on two lines could be driven by a gate output, since the loading is less than 100 pf. If the number of inputs to be driven were six and they were each three feet away, it would be necessary to buffer the gate output with a medium buffer (MB, Fig. 7) in order to drive the capacitive load.

The packaging concept used on Machines B and C limits the number of components per cubic foot to about 20,000, including the connectors and the back-plane wiring. There is now a full-scale development program underway at Burroughs to increase the packing density to over 20,000 components per cubic foot [12]. This test vehicle is due to be completed in about nine months. When finished, it will push the system performance of present transistor-diode circuitry closer to the breadboard limit of 50–60 Mc.

Conclusions

The hybrid transistor diode logic technique combines the advantages of lumped- and distributed-gain systems

maximum system flexibility and efficiency. Essenlly, this technique combines all of the following deable characteristics for a digital system:

1) Optimizes the use of the transistor, by its linear region usage, thereby permitting non-rigid requirements of specifications.
2) Achieves a minimum logical gate propagation time through the use of non-saturating, low-impedance circuitry.
3) Provides for large fan-in and fan-out capability.
4) Achieves maximum reliability through the use of a minimum number of required components.
5) Achieves optimum logical flexibility and signal distribution by optimum use of lumped- and distributed-gain systems.
6) Minimizes system cost through the use of diode gates and dual use of transistors as gates and buffers.

The speed of the system, in which these circuits are sed, is heavily dependent upon the packaging concept hich establishes the detrimental limits of inductive and apacitance loading upon the system.

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Esaki Diode Logic Circuits*

G. W. NEFF†, S. A. BUTLER†, MEMBER, IRE, AND D. L. CRITCHLOW†

Summary—The Esaki diode is a potentially low-cost, high-peed two-terminal device exhibiting a short-circuit-stable negative esistance over a portion of its volt-ampere characteristic. By proper asing and loading, it can be used to perform power amplification nd memory functions. In this paper, a variety of digital computer rcuits (a result of an early exploratory program) is described which ilizes the above properties. In particular, shift registers, triggers, nd counters are presented.

The following shift registers are described: 1) A register which onsists of one Esaki diode and one conventional diode per stage. hifting is accomplished with a two-phase square-wave drive. The saki diode provides memory and power gain, and the conventional ode provides a unilateral flow of information. 2) A register which ombines Esaki diodes with square-loop ferromagnetic cores. Again e Esaki diode provides memory and power gain. Upon application a single-phase drive, the cores perform a gating operation depend-g upon the state of the diodes. 3) With the use of Esaki diode-ansistor combinations, high-speed circuits are obtained which epend upon the Esaki diodes primarily for memory and the tran-stors for power gain and unilateral flow of information.

The flip-flop and counter circuits to be presented are the follow-g: 1) A binary counter using Esaki diodes with magnetic cores; 2) gh-speed flip-flops using Esaki diode-transistor combinations.

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INTRODUCTION

THE effectiveness of the Esaki diode as a computer device originates from its negative resistance characteristic. With appropriate bias and loading conditions, the diode can be operated in monostable, bistable, or astable modes as is common with all negative resistance devices.[1,2] However, the Esaki diode has several advantages over other negative resistance devices. The diode consists of a single junction, and the fabrication cost should be considerably lower than that of multijunction devices. Diodes are available which have a wide range of current ratings, varying from a few microamperes to several amperes, and the peak current adjacent to the negative resistance region can be accurately controlled through etching of the junction. The device is much less sensitive to temperature and radiation than semiconductor devices with lower impurity content. Furthermore, since the Esaki diode is a

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very low voltage device, and since low current diodes are available, the power consumption in switching circuits employing this device can be made small compared to present circuitry. The circuits discussed in this paper are the results of an exploratory program carried out in early 1959, the purpose of which was to generate possible applications of the Esaki diode in switching circuits. The intent was to investigate the diode properties and determine which of these properties would be useful in switching circuits and, further, to show how they could be used in combination with other nonlinear devices such as conventional semiconductor diodes, transistors, and magnetic cores.

The characteristics of the Esaki diode which are advantageous with respect to switching circuits are the existence of a threshold (which facilitates the performance of summation logic), power gain, the ability to perform binary memory, and the inherent high speed with which switching occurs. However, as the diode is a two-terminal device, switching circuits which contain it as the only nonlinear device are bilateral; in coupling such circuits to perform as a system, it is necessary to include a means of controlling the flow of information.

Logic Circuits Coupled with Linear Elements

The voltage-current characteristic of an Esaki diode is shown in Fig. 1(a). The load lines I–IV illustrate the various types of stability resulting from resistive loading. Fig. 1(b) shows a circuit driven from a current source. (The use of current bias as opposed to voltage bias is not essential, but will be used throughout the discussion for ease of description.) When considering the stable operating points of the various load lines, the point to the left of the negative resistance region will be referred to as the "low voltage state" or "0" state and that to the right as the "high voltage state" or "1" state.

In designing a system-oriented building block, it would seem preferable to use pure resistance loads on the Esaki diodes, both for low-cost and high-speed operation. The circuit of Fig. 2 shows a chain of Esaki diodes which are driven close to their negative resistance regions by a three-phase system of current sources. The current pulses applied to adjacent diodes have a region of overlap, during which time information is transferred. The coupling resistors R_T are such that the effective load on each diode results in bistable operation. The propagation time of the high-voltage state between adjacent diodes depends on circuit reactances such as lead inductance and diode-junction capacitance; to consider the diode load as purely resistive, the overlap time of the clock pulses must be long compared to this propagation time. A representative value for the propagation time is in the order of 1 to 2 mμsec for 5 ma diodes, with peak-to-valley ratios of 8:1. The net parallel resistance for simple transfer, driving from one to three loading stages, was 100Ω. The amount of current flowing from a diode in its high-voltage state to an

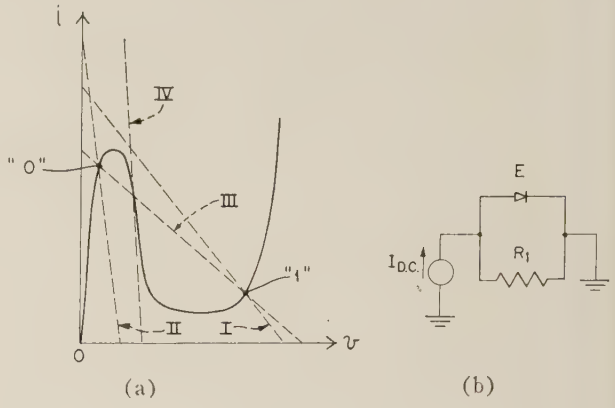


Fig. 1—Esaki diode circuit and characteristic showing various types of stability resulting from resistive loading.

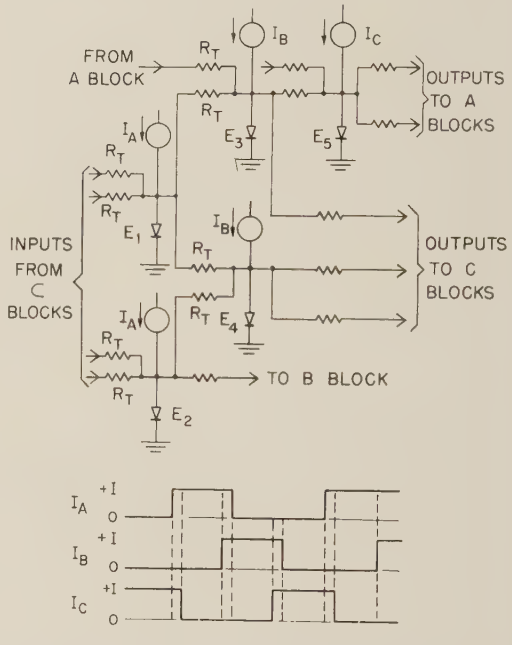


Fig. 2—Resistively coupled Esaki diode logic circuits. The transfer of information is from left to right under the influence of the three-phase overlapping clock system shown. Threshold logic is performed by each Esaki diode.

adjacent diode that is in the low-voltage state is determined by the coupling resistor R_T. By employing multiple inputs, summation logic can be performed giving rise to simple AND and OR circuits. Since the input lines to a circuit present a load after that circuit has switched, both input and output lines must be considered when designing for a bistable load line. This reduces the fan-out capabilities in proportion to the number of inputs.

The use of a three-phase drive system does not completely eliminate the problem of having a basic block that is not unilateral. A reverse flow of information may still occur during the time of overlap of two clock pulses. Referring to Fig. 2, assume that the circuits containing E_4 and E_2 are OR circuits, and that during A time, E_1 is in the "1" state and E_2 is in the "0" state. When clock pulse B is turned on, E_4 will switch to the

1" state which, in turn, will switch E_2 to the "1" state, hus providing an erroneous input to any other blocks iven by E_2. This problem of reverse flow can be elim- ated by providing temporary storage of information, nus eliminating the need for overlapping clock pulses. ig. 3 shows a system using inductors, along with the ock pulse waveforms that are required. For example, ssume E_1 in the "1" state when A is turned off. The nductor loading E_1 will maintain current flow through $_2$ and E_3 until B is fully on. The repetition rate will be mited by the L_T/R_T time constant.

The temporary storage produced by the inductors of ig. 3 can also be produced by capacitors. In this case, djacent blocks must be biased in the opposite polarity, naking it necessary to have the complementary pulses f the three-phase drive.

By using a clock system with rise times of the same rder as the propagation time between stages, the cir- uit reactances can provide the necessary temporary torage allowing a nonoverlapping clock system. The ircuit configuration is identical to that used in resist- nce coupling, but in this case the lead inductance and unction capacitance must be known and uniform for ach circuit. This system will allow a repetition rate of he clock system, which is a maximum of the two circuits iscussed thus far; to obtain higher repetition rates, the ssociated circuit reactances must be decreased.

The primary obstacle to the above-proposed schemes s the problem of tolerances on Esaki diodes, resistors, nd the clock systems. Calculations were made which ndicated that these schemes would impose severe toler- nce requirements and require a great deal of custom esigning for different conditions of logic functions and or different conditions of fan-in and fan-out. However, dvantages in fabrication techniques may alter this icture somewhat. Indications are that the diode char- cteristics can be controlled to an extremely high de- ree, and diodes with peak-to-valley current ratios of igher than 10:1 can be easily made.

Logic Circuits Coupled with Nonlinear Elements

The next group of circuits combines the Esaki diode ith a rectifying device as shown in Fig. 4. This results n amplifying and memory circuits having unilateral roperties, and allows maximum current gain with re- axed tolerance requirements and reduced power dissipa- ion. As before, monostable or bistable operation is vailable and when biased bistably, the "0" and "1" tates are as defined previously. Some examples of ap- licable rectifying devices are conventional rectifying iodes, zener diodes, low-voltage reverse breakdown iodes, and transistors. From Fig. 4 it can be seen that here is essentially zero current through the load when he circuit is in its "0" state, and that when in the "1" tate, the load receives a current approaching the dif- erence between the peak and valley currents of the saki diode.

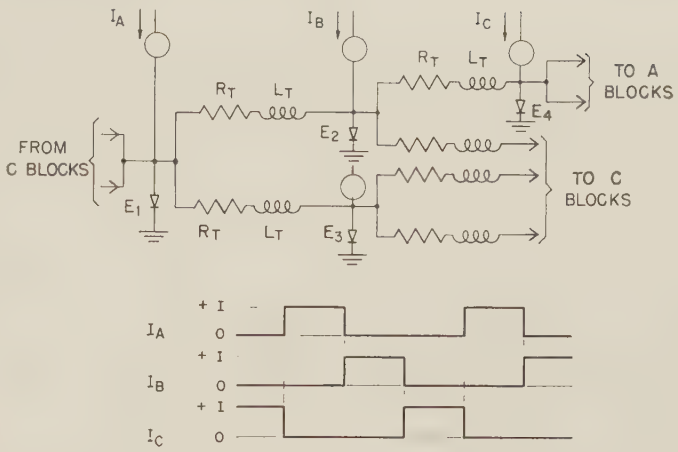


Fig. 3—Reactively coupled Esaki diode logic circuits. The inductors L_c provide temporary storage of information during transfer, allowing the use of a nonoverlapping three-phase clock system.

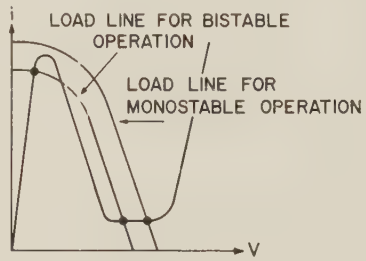


Fig. 4—Characteristic of Esaki diode showing nonlinear load lines.

In the circuit of Fig. 5, the unilateral property of an Esaki diode-rectifying diode combination is coupled with the temporary storage of an inductor to produce a shift register whose information flow is controlled by the two-phase nonoverlapping current drive also shown in the diagram. The current drive source is of an amplitude capable of biasing each Esaki diode-diode combination to its "0" state. At the termination of the clock pulse of any state, that stage is unconditionally reset. The current flow through a stage in the "1" state charges that load inductor coupling into the successive stage, so that when the clock pulses change, the successive stage will be forced to the "1" state by the addition of the clock current and inductor-discharge current. In this manner, the "1" state is shifted one position to the right at each reversal of the clock pulses. If the path D_n, L_n is connected back to node 1, an n-stage closed ring can be constructed. Because power gain is available, it is possible to have a multiple output from each stage of the shift register. Auxiliary outputs would serve as sources of driving a variety of low-level devices.

With the inclusion of a rectifying device in series with the load resistor across the Esaki diode, it is possible to achieve unidirectional flow of information in a resistively-coupled circuit. Here, as in the resistor-coupled case, each Esaki diode is current biased such that the parallel combination of the current bias and the load on the Esaki diode places its operation in a bistable

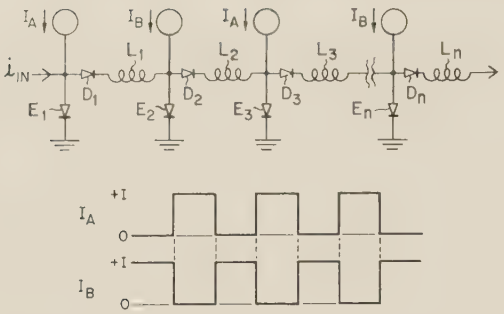


Fig. 5—Shift register employing temporary storage in inductors and rectifying action of conventional diodes to allow use of nonoverlapping two-phase drive.

region. Fig. 6(a) shows a circuit consisting of a chain of bistable Esaki diode-diode resistor circuits. If diodes E_2 and E_3 are in the same voltage state (high or low), there is little or no voltage across D_2; thus, D_2 is in a high resistance region. If E_3 is in a high-voltage state and E_2 is in the low-voltage state, D_2 is reverse biased and again is in a high-resistance region. The network D_2–R_2 need only be considered when E_2 is in the high-voltage state and E_3 is in the low-voltage state. Extension of the argument leads to the conclusion that output networks need only be considered when a circuit is in the high-voltage state, and input networks need only be considered when circuits are in the low-voltage state. This statement is true regardless of the number of inputs and outputs. This leads to the possibility of performing sequential AND and OR Kirchhoff logic, and, unlike pure resistance coupling, the fan-out capabilities are not limited by the number of inputs. To reset the circuit there are many possibilities, including logical reset via transistor devices capable of being driven from the Esaki diode circuits.

In Fig. 6(b) a bistable Esaki diode-diode resistor block is shown and a v-i characteristic is drawn with four different load lines. The load lines d, c, b, a, correspond to the conditions of three, two, one, and none of the circuits to the right is in the low-voltage state. The fact that a load is essentially disconnected when the diode switches to the high-voltage state can be used to good advantage to improve tolerances. For example, assume the circuit of Fig. 6(b) is loaded by two OR circuits and an AND circuit. The tolerance requirements on current input to AND circuits will be much more severe than for OR circuits. If OR circuits are designed to operate from the lower voltages (load line d) and AND circuits from higher voltages (load line b), then the OR circuits will switch first and the voltage will move to the higher and more constant value for control of the AND circuits.

Blocks of this type were tested for switching times using 5-ma diodes with ratios of approximately 8:1. The Esaki diodes were normally dc-biased at 4.0 ma. Transfer time was measured for cases of one-, two- and three-output stages. Each output stage was in turn

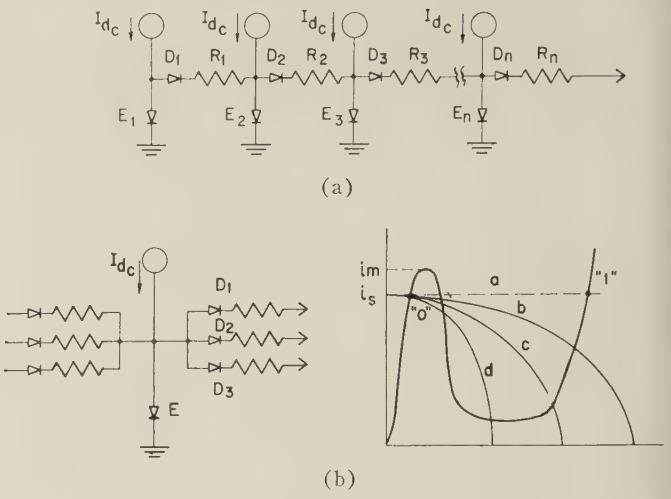


Fig. 6—(a) Logic circuit coupled with nonlinear elements. (b) Loading conditions on Esaki diode.

loaded with further stages. In all cases, the transfer times were in the range of three to five mμsec. Recovery time for the rectifying diodes used in the coupling networks was not considered, for until the over-all repetition rate of a system is determined, requirements for reset of any stage are unknown. However, with the use of fast recovery diodes, this recovery time should be compatible with the information transfer times. OR circuits, consisting of two- and three-input blocks, were tested, and again the transfer time ranged from three to five mμsec. Two- and three-way AND blocks were designed, which operated reliably with transfer times in the order of five to seven mμsec. A decrease in transfer time was accomplished in each case by increasing the dc bias to 4.5 ma. At this time, it would be premature to predict the ultimate feasibility of this approach.

The circuit shown in Fig. 7 is a subharmonic generator employing an Esaki diode and an inductor. A sinusoidal current source drives the diode in such a way that the swing from 0 to $+I$ is applied at A. The positive swing causes current to flow into the parallel combination of the inductor L and the reverse biased diode, causing a build-up of current in L. As the current swings back to zero, the current in L will decay, forcing current through the diode in the forward direction. Because of the dc component of the current source, the dc component of current through the inductor will increase upon successive cycles of the source, approaching the dc component of the source. The amplitude of the source and the value of R are such that after a certain number of cycles, the current through the diode during the return of the source to zero is sufficient to switch the diode to its high-voltage state. As a result of the increased voltage across L, the rate of change of current through L increases, and the dc component of current through L decreases. It requires several more cycles of the source to build this dc component up to a level capable of switching the diodes again. The test circuit built in the

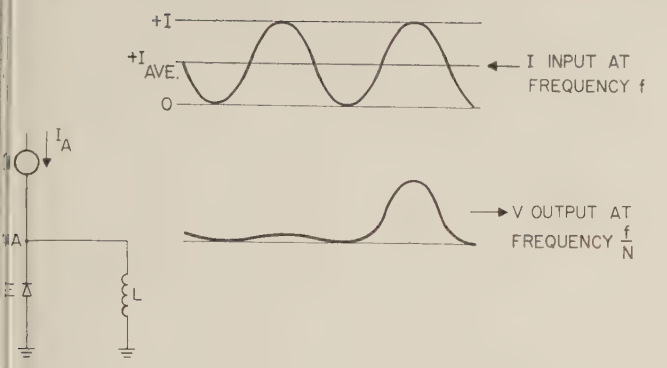


Fig. 7—Subharmonic generator utilizing Esaki diode and inductor.

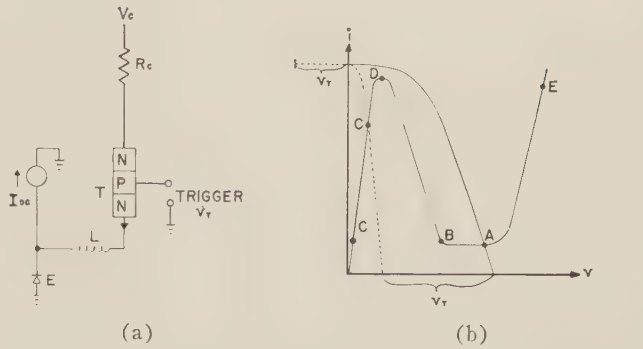


Fig. 8—Esaki diode operating in the emitter circuit of a transistor to provide current switching. The diode can be operated either monostably or bistably.

laboratory was capable of producing subharmonics up to the order six. This circuit was operated at 20 Mc.

Esaki Diode-Transistor Combinations

The following circuits serve to demonstrate that the Esaki diode may be used to good advantage in combination with transistors. Although these techniques would not cause the usage of Esaki diodes to approach that of transistors, they show that the device is presently a very useful and desirable circuit element.

The first circuits presented comprise a group in which the Esaki diode is placed in the emitter circuit of a transistor. In this type of operation, current is switched between the Esaki diode and the transistor. The Esaki diode is again current biased, and the emitter-base diode of the transistor presents a load on the Esaki diode, which is similar to that of the rectifying diodes previously discussed. It is possible, therefore, to switch current whose magnitude is almost equal to the current difference of the extremes of the negative-resistance region of the Esaki diode. Furthermore, triggering is accomplished with very low-level drive. Fig. 8(a) is a low-level pulse amplifier consisting of an Esaki diode in the emitter circuit of an *n-p-n* transistor. Fig. 8(b) is the *v-i* characteristic of the Esaki diode with the load line corresponding to the current source I and the emitter-base diode of the transistor. The inductor L is included to force switching of the diode to occur on a constant current path (*e.g.*, from point B to C). The normal operating point for the circuit is at A. The trigger voltage, V_T, can be any voltage greater than $V_a - V_b$ to initiate switching, and once initiated, the circuit will switch around the path A-B-C-D-E-A. If the trigger voltage V_T is greater than $V_a - V_b$, the operating point will remain at C' until V_T terminates, at which time it will go to D, switch to E, and then return to A. The triggering level can be made small by making the intersection point A close to the negative-resistance region of the Esaki diode. The amplifier is also pulse-width sensitive because of the charging time of the inductor L. If V_T has an amplitude greater than V_D but less than V_A and a pulse width greater than the period of the Esaki diode circuit, the circuit will oscillate at a frequency determined by L. Hence, the same configuration functions as either a dc or pulse-operated oscillator. There are several other interesting applications of this basic configuration which are achieved with minor changes in circuit parameters and triggering schemes. These include subharmonic generators and various bistable devices.

By placing the Esaki diode in the base circuits of transistors, the device may be used primarily as a memory element providing little or no current gain. The transistors provide the current gain necessary for a dc system. This approach results in simplified circuits with reasonable design tolerance requirements. The first circuit to be discussed, Fig. 9(a), is a high-speed (higher than 10 Mc) complementary set-reset trigger. The two Esaki diodes, E_1 and E_2 are dc biased by the current source I_{dc} and the resistors R_{E_1} and R_{E_2}. The current I divides between these resistors such that $I_{dc}/2$ flows through each diode in the forward direction. Fig. 9(b) shows the *v-i* characteristic of each diode with the dc load line, assuming the transistors to present no load. Each diode can exist in one of two states, *i.e.*, with the voltage v_1 or v_2 appearing across them. The state corresponding to v_2 is the ON state and that corresponding to v_1 is the OFF state.

Assume E_1 is ON and E_2 is OFF. Then the base of T_2 will be more negative than the base of T_1 by an amount $(v_2 - v_1)$. The Esaki diodes are chosen such that $(v_2 - v_1)$ is greater than the emitter-base drop of either transistor. Therefore, T_2 will conduct and T_1 will remain off. Now, if a positive current I of amplitude I_{dc} or greater is applied at the node marked Reset, it will essentially divide between R_{E_1} and R_{E_2}. Accordingly, a current of magnitude I or greater will flow through E_2 and zero current through E_1. From Fig. 9(a) it can be seen that the two diodes will switch states, making T_1 conduct and T_2 go OFF. Similarly, a current I into the node marked set will restore the initial state of T_2 ON, and T_1 OFF. If current is applied to the set condition while the trigger is in the set state, or applied to the reset position while the trigger is in the reset state, the state of the trigger will remain unchanged. It is important

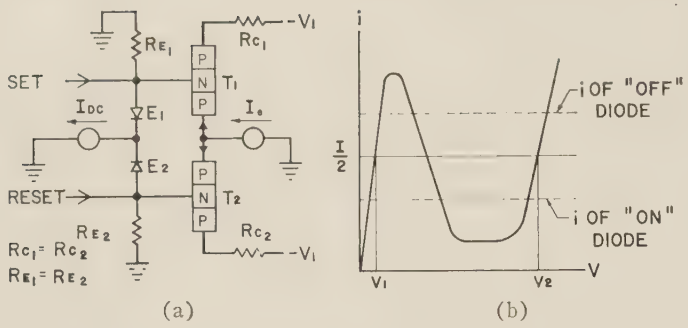


Fig. 9—(a) High-speed set-reset transistor Esaki diode trigger circuit. (b) Loading conditions on diode.

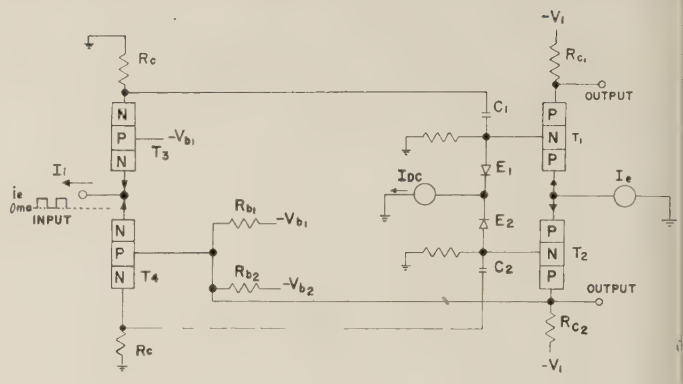


Fig. 10—Binary trigger formed from basic set-reset trigger of Fig. 9.

to point out that it is the difference in voltage across the diodes that determines which transistor conducts. Therefore, if the source I_{dc} is reversed, E_1 and E_2 can be reversed in the circuit. Furthermore, either *n-p-n* or *p-n-p* transistors can be used. High-speed operation is obtainable because of the very short switching time of the Esaki diode. The diode follows the input pulses only from their dc bias point to the negative-resistance region. Once this region is reached, the diode will switch with the speed which is characteristic of Esaki diodes, and the change of state of the trigger is a function of the switching characteristics of the transistors used.

The trigger described above can be enlarged to perform as a binary trigger. One means of accomplishing this is shown in Fig. 10. For the purpose of illustration, *p-n-p* transistors are used in the set-reset trigger (T_1, T_2) and *n-p-n*'s in the pulse-gating circuit which drives the trigger. Consider the set-reset trigger in the set condition with E_1 and T_2 on, and that I_i equals 0. Conduction of T_2 biases T_4 such that when I_i goes to the value i_e, T_4 will conduct. The conduction of T_4 charges C_2, causing a transient current to flow out of the reset input of the set-reset trigger. This current has the same effect as current into the set input and the state of the trigger remains unchanged. When I_i again goes to zero, C_2 discharges into the reset input of the trigger and the state of the trigger switches in the manner described above. Now T_1 is conducting and T_2 is OFF. With T_2 OFF. T_3 is conditioned to conduct, but conduction cannot occur because I_i equals 0. Again, when I_i goes to the value of i_e, T_3 conducts, charging C_1. The transient current resulting has the effect of a current into the reset input of the trigger, and the state is unchanged. When I_i returns to zero, C_1 discharges current into the set input, and the trigger state switches back to the set state, with T_2 conductive and T_1 OFF.

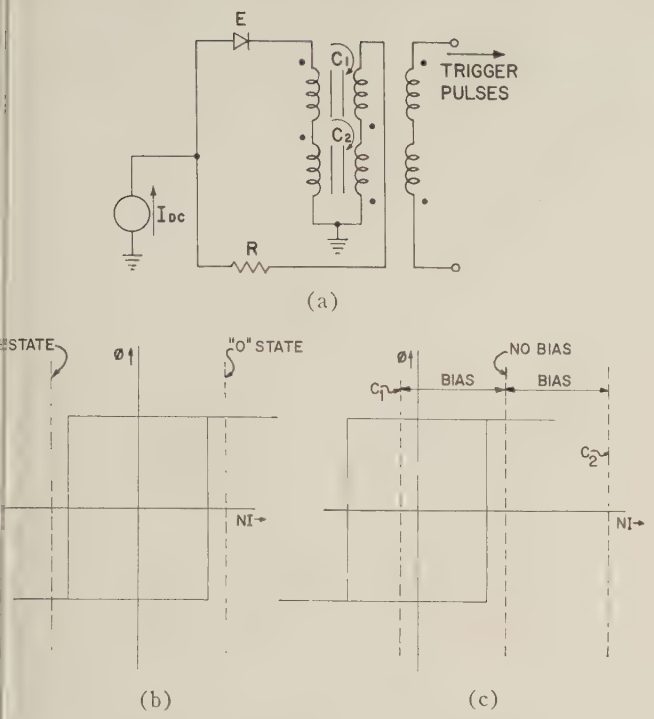
The circuit of Fig. 10 was constructed using drift transistors. The trigger functioned with input frequencies up to 15 Mc, with no particular optimization of design for speed. With careful design and adequate transistors, higher frequencies should be easily obtained.

Esaki Diode Magnetic Core Combinations

A variety of logic circuits such as shift registers and counters which utilize square-loop ferromagnetic cores have been developed within the last few years. These circuits are quite reliable; however, they require rather elaborate, and thus costly, pulse-driving systems. Two circuits are to be described where this core-driving function is performed by Esaki diodes. The first circuit is the binary trigger in Fig. 11. The resistor R and source current are chosen so that the dc load line of Case I in Fig. 1(a) results. Consider the case where the diode is in the "0" state. The diode current is larger than the resistor current, causing a net mmf on the cores which drives them into positive saturation, as seen in the ϕ-NI loop of Fig. 11(b). Upon application of a trigger pulse, the upper core is driven toward negative saturation, inducing a voltage and thus a current in the clockwise direction in the diode-resistor loop. This current switches the diode to the "1" state. (At this time the trigger pulse can be removed, if desired.) The resultant decrease in diode current and increase in resistor current causes the net mmf on the cores to be reversed, switching them to negative saturation. A stable dc operating point is finally reached with the diode in the "1" state. Upon application of another trigger pulse, a counterclockwise current is induced in the loop which switches the diode back toward the "0" state again. The current through the diode increases, reversing the mmf of the cores, thus switching them to positive saturation. A full cycle is completed when the dc operating point "0" is again reached.

Two features of the circuit should be noted. First, the polarity of the trigger pulse is not important. If the circuit is in the "0" state and a positive trigger pulse is applied, core 2 is switched by the trigger pulse while a negative trigger pulse would switch core 1. Secondly, the information storage in the circuit is performed by the diode; thus, flux remanence in the cores is not necessary. However, the saturation phenomena of the cores is a necessity.

It is advantageous in many cases to have a circuit which is sensitive to trigger-pulse polarity, *e.g.*, if one wants to make a multistate-binary counter. This circuit can be made polarity sensitive by a current bias through the trigger windings (or through windings in parallel with the trigger windings). The mmf's acting



g. 11—(a) Magnetic-core Esaki diode binary trigger. The circuit shown is sensitive to trigger pulses of either polarity. The application of a dc bias to the cores makes the circuit sensitive to pulses of only one polarity. (b) Operating conditions of binary trigger. (c) Biasing conditions on cores to make binary trigger.

ı each core are shown in Fig. 11(c) for the case in which ıe circuit is in the "0" state. Application of a positive igger pulse drives core 2 further into positive saturaon, while core 1 is driven along the steep back part of s ϕ-NI loop, inducing the clockwise current in the oop which switches the diode. If the trigger pulse were egative, the net mmf would not be large enough to vitch core 2, and as a consequence the diode would not e switched. If the circuit were in the "1" state, it would gain be switched only by a positive pulse.

The circuit diagram of a unidirectional transfer cirıit using Esaki diodes with square loop magnetic cores shown in Fig. 12. Three different modes of operation re possible corresponding to Cases I, II and III of Fig. (a). To explain this operation, assume that the dc oading condition of Case I prevails, and that all of the iodes are in the "0" state except for E_2, which is in the 1" state. Also assume that cores C_1, C_4, and C_5 are in ıe "0" state, *i.e.*, positive saturation.

There is less current flowing through E_2 than through ıe other diodes. This difference in current flows through ıe resistance R_2 and through the windings on C_2 and ₃, holding C_2 in the "0" state and C_3 in the "1" state.

Upon application of a shift pulse, a voltage is deeloped across the winding on C_3 that switches E_2 to the)" state and E_3 to the "1" state. The shift pulse can be emoved after the diodes have switched states. The ineased voltage across E_3 forces a current through the indings on C_3 and C_4, driving them to the "0" and "1" tates, respectively. Note that most of the energy for vitching the cores comes from the dc source. Diode E_3

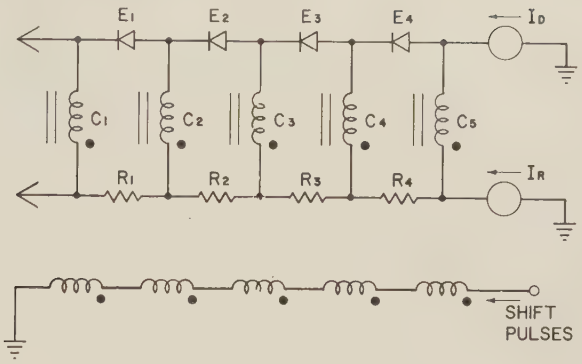


Fig. 12—Magnetic-core Esaki diode shift register. The saturable magnetic cores are used as storage and gating elements and the Esaki diodes provide power amplification.

remains in the "1" state after the cores have completed switching. The next current pulse shifts the information to diode E_4 and core C_5.

The difference in the value of current for points "0" and "1" is the amount of current available to switch the cores. The magnetizing current requirements of the core are such as to allow complete switching of the cores with this difference current. The voltage across a switching core forces a current through the adjacent core; therefore, the resistance must be large enough to prohibit this current from exceeding the threshold of the adjacent core.

The circuit of Fig. 12 can also be operated with the dc load lines of Cases II and III. For example, consider Case II. When a diode is switched to the high-voltage state a current is forced through the adjacent cores, thereby switching them. The cores being switched offer an impedance to this current that limits it sufficiently to keep the diode in the high voltage state. When the cores are completely switched, the current through them increases, and the diode switches back to the low voltage state.

Conclusions

The circuits described tend to point out the fact that the Esaki diode has desirable characteristics with regard to switching circuits. In retrospect, the particular characteristics that have been exploited are 1) the well-defined thresholds of the diode which allow the performance of summation logic, 2) the ability to perform binary memory and to provide gain, and 3) the high speed switching characteristics. These, coupled with the physical attributes of possible low cost and relative insensitivity to temperature variations and radiation, make the device appear to be of good potential value.

Acknowledgment

The authors wish to acknowledge the suggestions of H. S. Yourke in the investigations which produced the circuits described above. The contributions of Dr. H. N. Yu, J. F. Schomburg and Mrs. I. J. Eich, who provided a wide variety of diodes before they were generally available, are also gratefully acknowledged.

Tunnel Diode Logic Circuits*

R. H. BERGMAN†, MEMBER, IRE

Summary—The recent discovery of the tunnel diode with bandwidths extending into the kilomegacycle region has prompted investigation of their use in the logic and control portions of high-speed computers. Considerations of diode uniformity requirements, stability problems and power supply requirements has led to a monostable type of logical circuit. The switching properties of this circuit are analyzed and found to depend upon the negative resistance—capacitance time constant of the unit. The basic function performed by the circuit is a thresholding operation from which a set of logical building blocks is derived. Compatible dynamic and bistable storage schemes are discussed. Of major importance is the effect of diode variations upon the logical gains and delays of the circuits. These properties have been tabulated for tunnel diodes with 5 per cent tolerances on knee current and voltage. Experimental circuits using diodes with a time constant of 1.4 nanoseconds have given a nominal switching time of 7.5 nanoseconds.

Introduction

THE discovery of the tunneling effect in heavily doped semiconductor junctions has led to an appreciable amount of effort in the development of the tunnel diode. Early work in this field,[1] the extremely high cut-off frequencies that have been obtained with the units to date, and the predictions of even higher bandwidths[2] have suggested their use as elements in high-speed computer circuits. This "breakthrough" in high-speed semiconductor technology coupled with the simplicity of the device and its stability make it a prime candidate for computer application.

In order to satisfy the requirements for the logical and control portion of a computer, a set of logical building blocks is required. Normally associated with the logical building block is some means of signal amplification or fan-out, and signal standardization. In addition to the logical circuits, a compatible storage device is useful. The most critical requirement in the logical building block is for amplification, since the other functions may be performed by passive elements. As speed requirements are increased, the number of types of active elements that have an adequate gain-bandwidth product becomes the limiting factor in selection of the building block.

Two methods of amplification are possible with the tunnel diode: linear and regenerative. The two methods are illustrated in Fig. 1 on the static characteristics of a typical tunnel diode. For linear amplification an operating point is established in the most linear region of the negative resistance portion of the characteristics (point A) by the load line r_1 and the dc bias voltage V_1. The resulting circuit is also shown in Fig. 1.

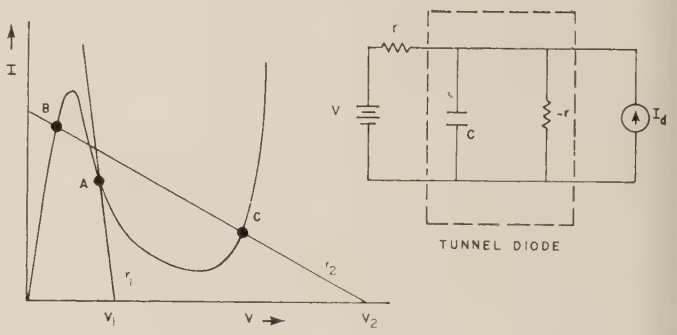


Fig. 1—Operating modes with tunnel diode.

If a small signal is applied from a constant current source, it is amplified by the factor

$$\frac{|-r|}{|-r|(1+j\omega Cr_1)-r_1}$$

where $r_1 < |-r|$, in order to establish a singular stable operating point. Notice that as the signal amplitude is increased and the operating point swings into the higher negative resistance regions of the tunnel diode, the gain of the circuit decreases and provides signal limiting. Two disadvantages of this circuit as a pulse amplifier present themselves. First, examination of the requirements for stability of the circuit indicates that series lead inductance must be kept extremely small. For stability the maximum series lead inductance is given by:

$$L_s < Cr_1|-r|$$

where C is the capacitance of the tunnel diode plus any additional shunting capacitance. For example, if $C = 100$ pf, $|-r| = 8\Omega$ and $r_1 = 4\Omega$, then L_s must be smaller than 3.2 nanohenries. The other disadvantage is the requirement for a linear and stable region in the negative portion of the diode characteristics. This requirement arises from the sensitivity of the gain of the circuit to changes in negative resistance.

The regenerative, or switching mode of operation, is obtained by increasing the load line to r_2 and the voltage source to V_2. This load line intersects the diode characteristic in three places; however, only points B and C are stable operating points. If the circuit is at point B and a positive current step of sufficient amplitude is applied, the operating point will switch to point C. Correspondingly, a negative input signal will switch it back again to point B. This switching mode of opera-

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[1] L. Esaki, "New phenomenon in narrow Ge *p-n* junctions," *Phys. Rev.*, vol. 109, pp. 603–604; January 15, 1958.

[2] H. S. Sommers, Jr., "Tunnel diodes as high-frequency devices," PROC. IRE, vol. 47, pp. 1201–1206; July, 1959.

n is differentiated from the linear mode in which the put signal is a linear function of the input. In the tching mode a thresholding operation is involved, ere only input signals greater than the threshold will se switching. The switching mode is also nonre- sible in action; that is, if the threshold is exceeded circuit will switch to the high voltage state C and y there regardless of whether or not the input signal ains. Therefore, it has memory.

An inherent advantage of the switching mode of op- tion is its nonsensitivity to the exact linearity or pe of the negative resistance region of the tunnel de characteristic. Slight irregularities in the nega- e resistance characteristic will have a negligible effect the switching action. Amplitude standardization is obtained in the switching mode by the diode char- eristic in the positive resistance regions, since the cir- t will switch to the relatively constant voltage high te regardless of the amplitude of the input signal. Gain may be obtained in the switching circuit by ad- ting point B so that it is near to the current threshold he diode characteristic. Then a relatively small input rent can be used for triggering. Once switching to nt C has occurred, considerably greater current is ilable to the load.

Since static storage is not desired in a basic logical ment, some means of returning the circuit to the ginal operating point B is desirable so that repetitive ical functions may be performed. The circuit of Fig. 2 forms this function by virtue of its single monostable erating point E.

Basic Monostable Circuit

In the monostable circuit of Fig. 2, the static load e is determined by resistance R_0 and voltage V_0. If is less than the minimum dynamic negative resist- ce of the diode, there will be only a single operating nt. Furthermore, if V_0 is adjusted so that the operat- point E is established below the current knee of the aracteristic, the circuit will be stable. The dynamic d line is determined by the inductive time constant R_0; and for cases where this time constant is long mpared with the switching time of the diode, the namic load line is essentially one of constant current. If a small step of current, (I_{in}) is applied to the diode shown in Fig. 2, the operating point will switch the high voltage point F along the constant current th shown. Removal of the input will cause the operat- point to move to F'. At this point the energy stored the inductor must be dissipated before the circuit return to its original operating point. As the energy the inductor decreases, the operating point moves ng the diode characteristic to the point of minimum rrent, G. Upon reaching this point, switching occurs ce again along a constant current path to point H. e cycle of operation is completed by a recovery ion where the energy in the inductor builds up to original level. During this buildup the operating

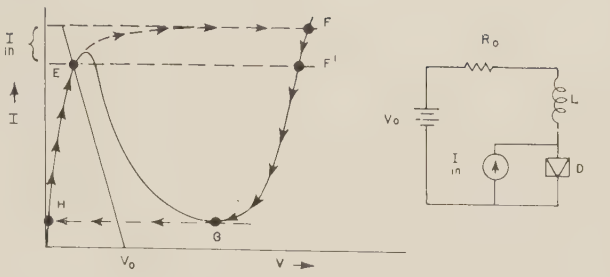

Fig. 2—Monostable circuit.

Fig. 3—Diode voltage waveform for monostable circuit.

point moves up the diode characteristic to the starting point. The waveform resulting from this cycle of operation is shown in Fig. 3. Because the circuit switching action is controlled by its inductance, the output waveform contains essentially no dc component, and may be ac coupled without requiring dc restoration.

Switching Characteristics

In order to calculate the switching characteristics for a tunnel diode monostable circuit, analysis of the simplified equivalent circuit of Fig. 4 is required. The elimination of the inductive biasing network from the equivalent switching circuit is justified when the inductive time constant of the biasing network is large compared with the switching time of the circuit. In Fig. 4, C is the tunnel diode capacitance plus stray capacitance; R_L is the total load, composed of the parallel combination of all input and output loads; R_D is the resistance of the tunnel diode, which varies as a function of its voltage; and I_{in} is a current step approximating an input from a driving gate. The resistance of the tunnel diode, R_D, in its various voltage ranges is nonlinear. Many linear and higher order approximations of the voltage-current relationships of the tunnel diode may be made depending upon the accuracy required in the particular problem. For this case, the characteristic has been approximated by linear resistances in four separate voltage ranges as shown in Fig. 5. In general, the characteristic of the diode in any voltage range may be approximated by a linear resistance either shunted by a current source, I_D, or in series with a voltage source, V_D.

Typical relationships for the resistances, referenced to the operating point A are

$r_4 = r_1$ shunted by a current source of magnitude;
$I_D = I_{max} - I_{min} - I_1$,
$r_2 = -1.6\, r_1$ shunted by a current source of $I_D = -I_1$,
$r_3 = \infty$ shunted by a current source of
$I_D = I_{max} - I_{min} - I_1$,

where

$$I_1 = V_1/r_1.$$

For a typical bias point, A would be located so that $I_1 = I_{max}/20$. If $I_{min} = I_{max}/6$, then:

$$V_1 = I_{max} | r_2 | /33,$$

$$V_2 = | r_2 | (I_{max} - I_{min}),$$

$$V_3 = 2 | r_2 | I_{max},$$

$$V_4 = 0.6 | r_2 | (I_{max} - I_{min}).$$

Therefore, the complete static characteristic of the diode may be described in terms of the knee current, I_{max}, and the negative resistance, r_2.

Solution of the differential equation

$$C \frac{dV_D}{dt} + \frac{V_D}{R_T} = I(t)$$

is required to determine the switching properties of the circuit. Here R_T is the parallel combination of the diode resistance and the load resistance. The solution to this equation is:

$$V_D(t) = I_{TOT} R_T (1 - e^{-t/R_T C})$$

where I_{TOT} is the sum of the input current I_{in}, and the equivalent current source I_D in the appropriate voltage range. When R_T is positive, the time required to traverse a particular voltage range V_p is given by

$$t_p = R_T C \ln \frac{I_{TOT} R_T}{I_{TOT} R_T - V_p};$$

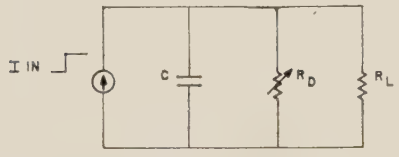

Fig. 4—Simplified equivalent monostable circuit.

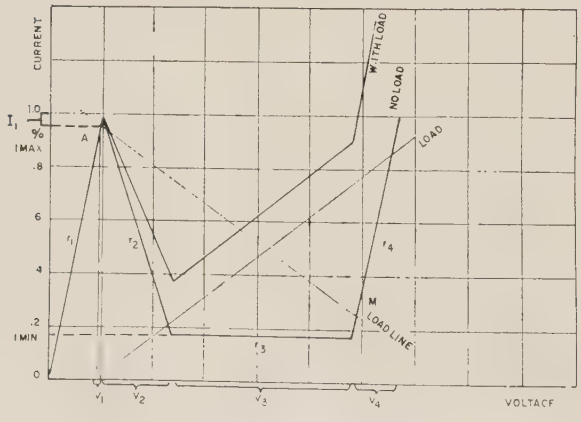

Fig. 5—Approximate diode characteristic.

where R_T is negative, the time is given by

$$t_n = R_T C \ln \left(1 + \frac{V_p}{I_{TOT} R_T}\right);$$

and where $R_T = \infty$, the time is given by

$$T_\infty = \frac{V_\infty C}{I_{TOT}}.$$

Fig. 6 shows a calculated normalized curve of switching time vs input current for a circuit with no loading. The switching time is expressed in terms of the time constant r_2C, and the input current in terms of percentage of the knee current, I_{max}. Included in Fig. 6 are experimental points for a diode having a time constant of 1.2 nanoseconds.

To determine the effects of loading upon switching speed, it is first necessary to determine the effects of a given load upon the characteristic of the diode. Since the load is in parallel with the diode, the composite characteristic of the two is such that the current at a given voltage is the sum of the individual load and diode currents at that point. A load, referenced to static bias point A, is shown in Fig. 5 and the composite characteristic has been drawn. The load has been selected so that its current is $\frac{3}{4} I_{max}$ when the circuit switches to the high state. The value of this load is $3.8 | r_2 |$. A load of this magnitude represents the approximate maximum allowable loading with relatively constant output voltage. Greater loading will cause a considerable reduction in output voltage during switching due to the abrupt change in the diode characteristics as the operating point moves closer to the valley. The switching time with this load is calculated as before with the composite characteristic used to determine the resistance and equivalent current source in the various voltage ranges. The results are plotted on Fig. 6.

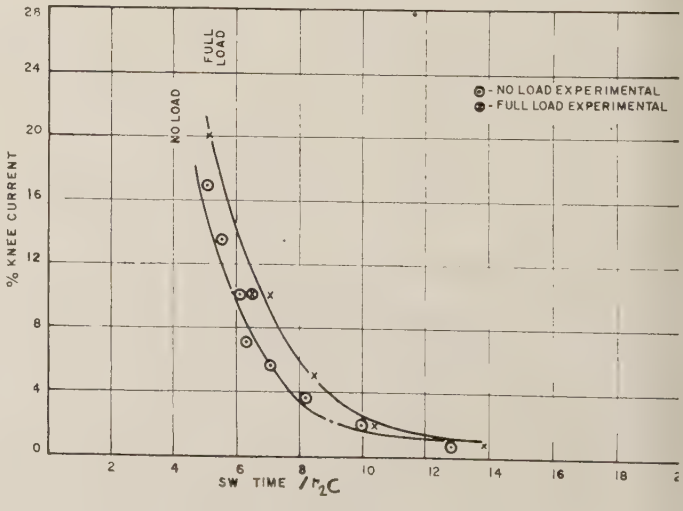

Fig. 6—Switching characteristic.

The voltage switching waveform is shown in Fig. 7. his waveform can be divided into four regions that rrespond to the four linear voltage regions of the diode aracteristic (Fig. 5). Region one corresponds to the ne required for the operating point to reach the knee the characteristic. When the input is greater than the ee by a very small amount, this time can become apeciable. As the input is increased, this time interval creases. Region two corresponds to the time required r the operating point to move through the negative sistance region. When the input is small, the switching tion begins slowly and a considerable delay occurs fore any appreciable voltage change occurs. In region ree, the diode impedance is high and the rate of voltage ange is constant. In region four, the diode impedance low and limits the voltage swing. In general, the itching action may be divided into two separate rts. The first is a delay in time corresponding to that quired for the operating point to move over the diode ee. The length of delay is dependent upon the amplide of the input triggering signal. In the delay region appreciable change in output voltage occurs. The cond part is the output voltage rise corresponding to e operating point moving across the valley of the ode characteristic. The time required to traverse this rtion of the characteristic is relatively independent the input triggering amplitude and depends mainly on the time constant of the diode used. This indendence of output rise time with respect to triggering nditions means that there will be no deterioration of lse rise time as a signal travels through a long string gates. Fig. 8 is a composite photograph of the switchg action of a series of gates taken with a sampling osilloscope. The time scale is 5 nanoseconds per major division. The first pulse is the input which has a faster rise me than the tunnel diode. The rise time of the first te is slightly faster than the succeeding gates; however, after passing through the second gate no additional deterioration is noticeable. The diodes used had an average time constant of 1.4 nanoseconds.

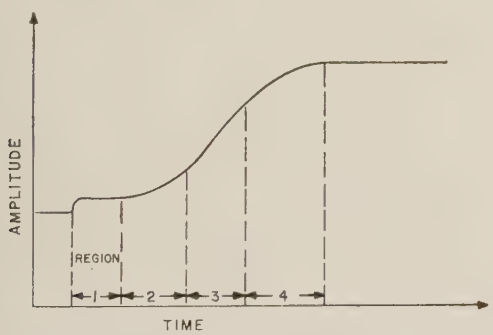

Fig. 7—Diode voltage switching waveform.

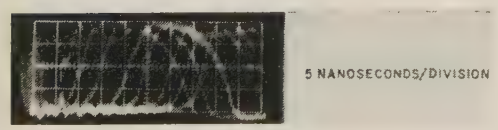

Fig. 8—Switching action of a series of gates.

Recovery Time

In order to determine the length of time that the circuit remains in the high state after triggering, and the length of the recovery time after switching back to the low voltage state, the circuit of Fig. 9 must be considered. (In this circuit the diode has been approximated by its equivalent voltage source, V_D, and resistance, R_D, shunted by capacitance, C_D.) The current through the inductance is of the form

$$I_L(t) = K_0 + K_2 e^{-\alpha_1 t} + K_3 e^{-\alpha_2 t}$$

where K_0 is the change in current required for charging or discharging the inductor, and α_1 and α_2 are the roots of the characteristic equation. The roots are given by

$$\alpha_1, \alpha_2 = \frac{R_0}{2L} + \frac{1}{2R_D C_d} \pm \sqrt{\left(\frac{R_0}{2L} + \frac{1}{2R_D C_d}\right)^2 - \frac{1}{LC_d}\left(1 + \frac{R_0}{R_D}\right)};$$

for typical circuit values

$$\frac{1}{LC_d}\left(1 + \frac{R_0}{R_D}\right) < \left(\frac{R_0}{2L} + \frac{1}{2R_D C_d}\right)^2$$

and

$$\frac{R_0}{L} < \frac{1}{R_D C_d};$$

therefore, α_1, α_2 may be approximated by

$$\alpha_1 \cong \frac{1}{R_D C_d}, \qquad \alpha_2 \cong \frac{R_0 + R_D}{L}, \quad \text{and} \quad K_2 < K_3.$$

The recovery of the inductance is therefore determined primarily by the time constant $L/(R_0+R_D)$. Calculations based on the simplified equivalent circuit of Fig. 10 are justified on this basis. During the recovery region where the current is building up to that of the bias point,

$$V_0 \cong I_{\max} r_1,$$
$$R_D = r_1,$$
$$V_D = 0,$$
$$I_{L0} = I_{\max}/6,$$

where I_{L0} is the initial current in the inductor, and the time required for the inductor to charge up to its static value may be approximated by three charging time constants,

$$\tau_{\text{rec}} \cong 3 \frac{L}{R_0 + r_1}.$$

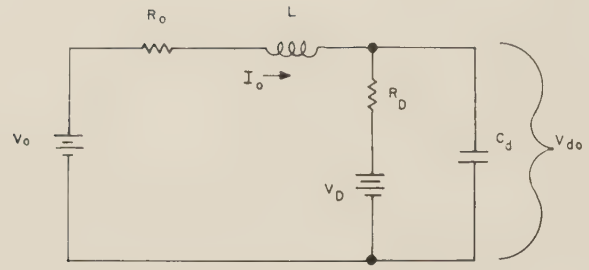

Fig. 9 Equivalent circuit for recovery time.

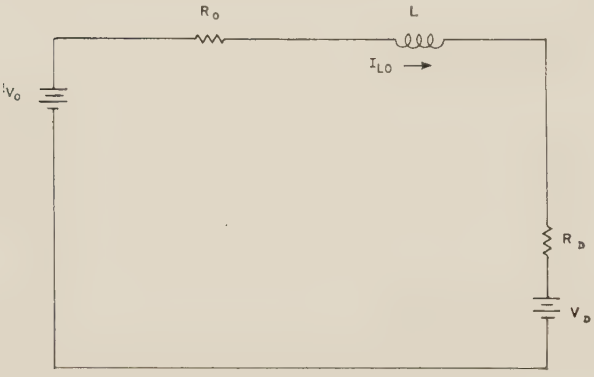

Fig. 10—Simplified equivalent circuit for recovery time.

When the circuit has switched to the high voltage state

$$V_0 \cong I_{\max} r_1,$$

$$V_D = I_{\max} r_1 + V_2 + V_3 - \frac{r_1 I_{\max}}{6},$$

$$R_D = r_1,$$

$$I_{L0} = I_{\max}.$$

The total current change through the inductor under these linear conditions is the sum of the initial current and final current values. The final current for an assumed linear system is determined by the ratio

$$I_{\text{final}} = \frac{V_D - V_0}{R_D + R_0}$$

and the total current change is

$$I_{\text{TOT}} = \frac{V_D - V_0}{R_D + R_0} + I_{\max}.$$

The actual current change is given by the difference between the initial current and the current at which the linear approximation no longer holds and is

$$I_{\text{actual}} = I_{\max} - I_{\min}.$$

The time required for this current change to occur is determined by a transient analysis of the circuit of Fig. 10 and is given by

$$t_{\text{on}} = \frac{L}{R_0 + R_D} \ln \left(\frac{I_{\text{TOT}}}{I_{\text{TOT}} - I_{\text{actual}}} \right).$$

Expressed in terms of diode parameters, the "on" tim is given by

$$t_{\text{on}} = \frac{L}{R_0 + r_1} \ln \left(\frac{6R_0 + 24r_1}{R_0 + 19r_1} \right).$$

For a source impedance R_0 equal to r_1, the ratio of "on time to recovery time may be calculated. This ratio i given by

$$\frac{t_{\text{on}}}{t_{\text{rec}}} = \frac{0.2L/r_1}{1.5L/r_1} = \frac{.1}{7.5}.$$

Logical Circuits

The basic method for triggering the monostable ci cuit into its cycle of operation is to provide an input sufficient amplitude and duration to drive the tunn diode into the region where it exhibits a negative r sistance and will continue its cycle unaided. Since th shape of the characteristic at the current knee indicat a very abrupt change in dynamic resistance from a lo positive to a low negative resistance, a rather well-d fined threshold is established. Only inputs which exce this threshold will trigger the circuit. If a standard inpu current to a circuit is adopted by assuming consta voltage swings for triggered gates and fixed couplin impedances between gates, a logical threshold functic can be performed. For example, if the static operati bias is adjusted so that one input of an N-input gate required to exceed the threshold, an OR function performed. Similarly, if all inputs are required to e ceed the threshold, an AND function is performe Since the coupling impedance is high compared to t diode impedance the inputs can be considered as cu rent sources during the period that the threshold operation is being performed. Fig. 11 shows a thre input AND gate with proper biasing point and cu rent inputs. By a slight increase in the operating poi bias the circuit may be made to trigger on two of i three inputs. The logical function now performed is "Majority."

To complete a set of logical functions, negation or i hibition is required. The basic circuit operation tha provides these functions is signal inversion. In vacuu tube and transistor circuitry, inversion is inherent the basic operation of the devices. Since the tunnel dio is a two-terminal device no inversion is provided in t device itself and it, therefore, must be performed by t circuit. The use of a transformer to perform this fun tion is shown in Fig. 12. The transformer replaces the i ductance of the original circuit and provides a 1-to inversion. In order for the timing of the cycle of oper tion to remain constant, the transformer has an add tional requirement of controlled primary inductance the same value as the inductor it replaces.

Since the transformer replaces the inductance in t circuit, its time constant determines the length of t

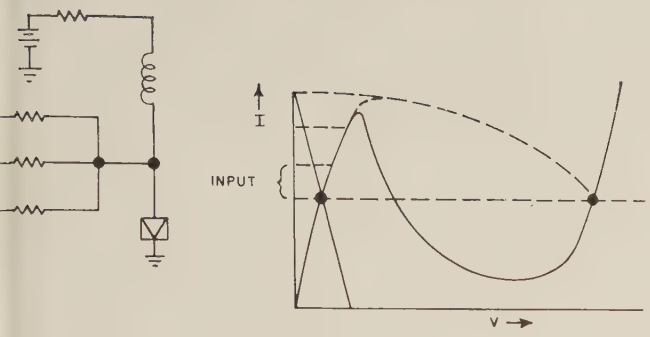

Fig. 11—Input AND gate.

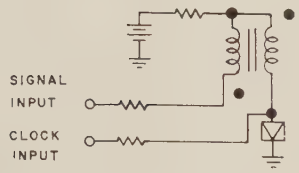

Fig. 12—Inverter using a transformer.

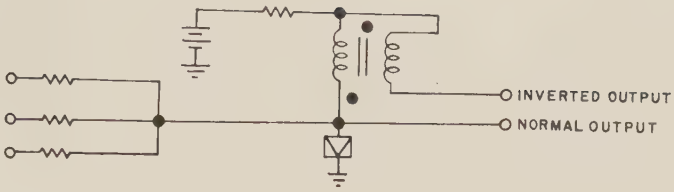

Fig. 13—Logical building block.

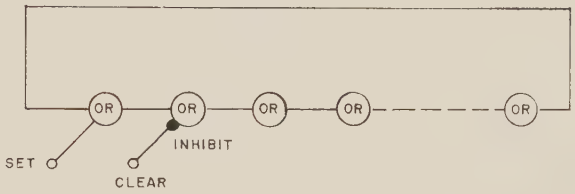

Fig. 14—Dynamic storage loop.

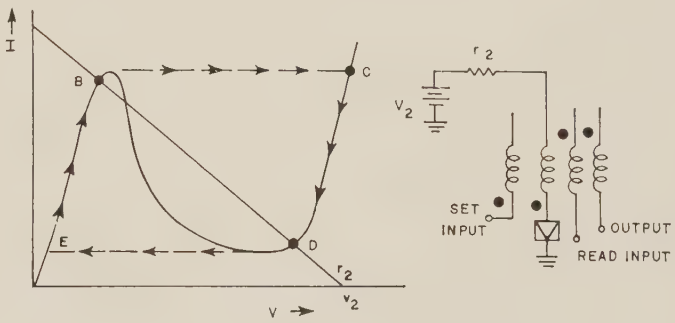

Fig. 15—Bistable storage element.

peration cycle after triggering. Therefore, there are no dditional recovery problems involved due to variations pulse rates through the transformer. Negation is per-rmed by inverting the signal through a transformer nd using this inverted output to cancel or inhibit an R gate which is driven by a clock pulse with appro-iate timing. Any logical signal may also be inhibited a similar manner. A single logical building block may e constructed as in Fig. 13. The inputs to the gate rm an AND, and either normal or inverted outputs e available. All logical functions may be generated ith such a circuit.

orage

With a set of logical operators, some form of com-atible information storage is usually required. The ype of storage employed is normally dependent upon he basic logical circuit configuration. For dc coupled synchronous transistor logic, a bistable storage ele-ent is normally employed. For dynamic circuitry, a ynamic storage loop of fixed delay is commonly used. nce the basic monostable logic circuit considered here dynamic, a dynamic storage scheme was considered. uch a storage method would consist of a series of gates onnected in a closed loop with some means of reading formation into and out of the loop. Fig. 14 shows one ossible scheme. The total number of gates required in he loop is dependent upon the ratio of the gate delay cycle time. If this ratio is $1/m$, then a minimum of gates must be cascaded to store one bit of information. o reduce the required number of gates, passive delay ements may be utilized if space and cost requirements dictate.

Where m is large, a bistable form of storage may prove ore economical. A bistable storage element is shown in Fig. 15. Bistability is obtained by increasing the source impedance, r_2, and voltage V_2 so that static operation at points B and D is possible. Due to the transformer inductance, switching occurs as in the monostable circuit along the constant current paths BC and DE with recovery times following the switching action until the new static operating point is reached. To switch from the low voltage to the high voltage state, a positive input trigger current is required; while a negative trigger is required to switch back to the low voltage state. Correct polarity for switching action is determined by the winding sense of the transformer. After switching and before recovery by the transformer, an output signal is available at the output winding of the transformer which is used to drive other logical circuits.

When the circuit switches in the opposite direction back to its original state, a negative signal appears at the output. This negative signal will not trigger the succeeding logical circuits. Typical operation of the circuit as a storage element would be as follows: Two inputs are provided, a set input and a read input; and an output is available. When the bistable element is in the low voltage state, a zero is stored; when it is in the high voltage state, a one is stored. The set input triggers the diode to the high state where it remains holding the

stored bit until reset. The switching action is inverted through the output winding so that a negative output occurs during the setting operation. A read input is inverted through the transformer and resets the element to the zero state. The negative switching action is inverted through the output winding and triggers the following logical circuits. If the element happened to have a zero stored, the read input would not switch the element and a signal would not appear on the output winding. Since the reading process is destructive, a recirculation path is required to maintain the information. Two bistable elements may be operated in a two-phase storage scheme as shown in Fig. 16. Reading may be done at periodic intervals by clocking signals or may be under the control of logical signals.

Standard monostable gates are used between the two bistable elements to provide sufficient gain for fan-out and to insure directionality.

Directionality Requirements

Investigation of the operation of an OR or a threshold gate reveals that all inputs need not be high to trigger the gate. Since inputs and outputs are common to the gate, the inputs which are not high during this triggering action will act as loads if the coupling elements between gates are bilateral. In this situation, false triggering of some gates is possible. To prevent such action, a directional coupling element is required. The use of a directional diode as the coupling element satisfies the basic requirement of providing directional isolation due to the difference in forward and reverse impedance. Also, directional diodes are available which are extremely fast and therefore compatible with the speeds obtainable with tunnel diodes. An additional requirement for the coupling element is that it must present the proper forward impedance required by the characteristics of the tunnel diodes used. Also, this forward impedance must be obtained with the signal voltage swings available from the tunnel diode. If the signal swings are not adequate, a forward biasing scheme as shown in Fig. 17 may be employed. No additional components are required for this scheme; however, one additional bias voltage is needed. Recovery requirements for the coupling diode are worst when an input is high and conducting during one cycle of operation and low during the next. In order to provide reverse isolation, the diode must recover in the recovery time of the tunnel diode circuit.

In situations where all inputs to a gate must be in the high state for triggering to occur, such as in an AND gate, directional coupling is not required and resistance coupling may be employed. In this case, one must worry about the effects of the inputs upon the total fan-out capabilities of the gate. Examination of the sequence of events in the triggering of an AND gate indicates that loading caused by the inputs to the gate does not

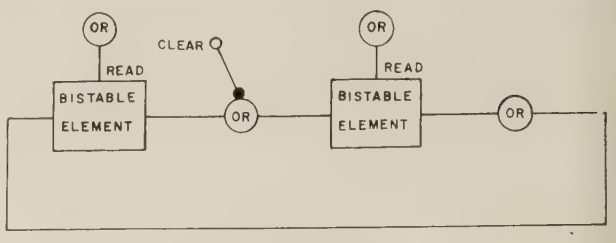

Fig. 16—Bistable storage.

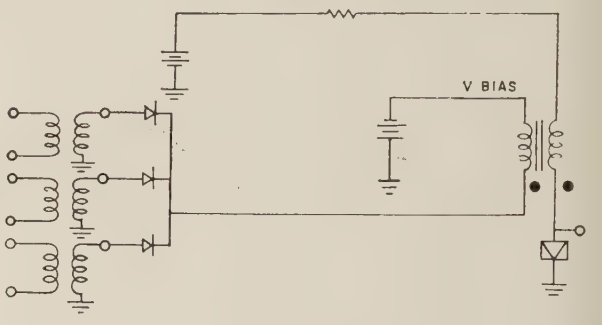

Fig. 17—Biased OR gate.

occur at the same time as the loading caused by t driven elements. This may be demonstrated by follo ing through a cycle of events involved in the operati of an AND gate. First, all of the inputs to the gate a triggered to the high state so that trigger current supplied from all inputs to the gate. One gate del later, or the time required for the gate in question to r spond to the high state, the gate is in its high-volta state and is delivering current to its loads. If a synchr nous logical system is used, the gate will have trigger those of its loads that are required to switch by the lo cal configuration, within one or two gate delays. At th point, the gate has performed its function and must nc recover for the next logical operation. Notice that this time the inputs to the gate are still high. This is d to the fact that a "one" is represented by a pulse that in the high state for "several" gate delays. Due to t sequential nature of the events, the input gates will r cover first and place an additional load upon the gat This load occurs one gate delay before the circu switches to the low state and does not disturb the logi

Logical Gain

Logical gain or fan-out is the number of similar gat that a gate can drive. The speed of operation of a lo cal system is in general determined by the delay of i individual gates, the number of inputs, and by the lo cal gain available from the gates. This is particular true in parallel logical schemes, where a large numb of gates must be driven at each logical level.

In the tunnel diode circuit considered, the logical ga is determined by the total current available when a ga is in the high state and the individual input currents r

red by the loading gates. Fig. 5 shows the effect of a istive load placed across a tunnel diode circuit. The d that a gate presents consists of its coupling im- lance in series with the diode in its biased condition. ce the coupling impedance is high compared to the de impedance, the input impedance can be approxi- ted by the coupling impedance in series with a volt- source equal to the biased voltage, V_0. A full load n would consist of the input impedance of n gates in allel returned to the biased voltage, V_0, where n is logical gain of the circuit. Examination of the effects variation of load impedance indicates that the itched voltage decreases as the load is increased. If ximum load is chosen so that the high voltage point which the circuit switches is above the valley of the racteristic point (*e.g.*, M in Fig. 5), the percentage nge in output voltage with loading can be kept below per cent. This maximum loading corresponds to a d current, I_L, of 75 per cent I_{max}, with the remaining rent flowing through the diode. This restriction on ding and output voltage variation also places a limit the maximum valley current that can be tolerated. r the figures quoted above, the minimum ratio of ax to I_{min} is about six to one.

When the operating point is lowered as it is in the ND gate to I_{AND}, the maximum loading that can tolerated is reduced, in order to meet the same re- irements of output voltage variations.

The input current requirement may be divided into o separate parts: the current required to overcome riations in diodes, power supplies, output voltage, and upling elements; and the current required to switch e gate with the chosen delay.

Once the maximum individual current requirements ve been determined, they may be summed up to give e total input current required per gate. The logical in can then be calculated by the ratio of the total d current available to the input current requirement. Assuming that an input current of 7.5 per cent I_{max} s been selected to provide the maximum gate delay owable, that diode knee variations do not exceed 5 per cent, and that power supply variations do not ceed ± 2.5 per cent, the current required to overcome ese variations may be calculated graphically. Fig. 18 ows extreme cases of diode knee characteristics and e corresponding worst case load lines required for an R gate, and a two-input and a three-input AND te. The voltage source impedance is $r_{1/3}$. In the case the OR gate, the minimum input current that must provided per input is equal to 11 per cent I_{max}. For e two-input and three-input AND gates 15 per cent d 20 per cent I_{max} are required respectively. The upling impedance required for each gate is deter- ned by the ratio of the minimum output voltage to e minimum input current requirement. The maximum tput current available for each gate is determined by

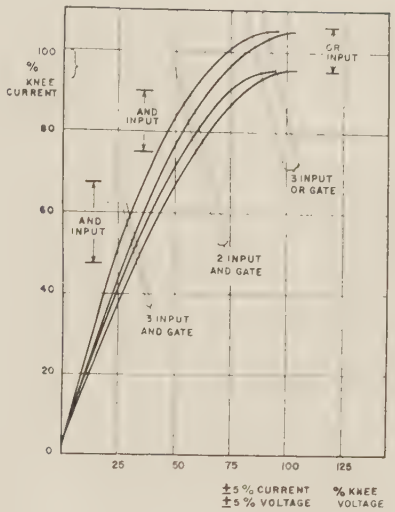

Fig. 18—Gate biasing.

the difference between the minimum operating bias current and 25 per cent I_{max}.

Once the tolerances have been determined for the diodes and related circuitry, it is possible to calculate the maximum and minimum switching times for each gate. For example, the maximum switching time occurs for the OR gate when only one input is present, the gate is fully loaded, and tolerance variations are at an extreme so that the amount of input current in excess of the knee is only 7.5 per cent. Under these conditions the switching time is 7.4 r_2C. The conditions for minimum switching are that all three inputs are present, loading is minimum, and tolerance variations are such that a maximum amount of the total input current is available for switching. Under these conditions, the switching time is 4.4 r_2C. In Table I, the properties

TABLE I

Logical Function	No. Inputs	Logical Gain Standard Loads	Input No. Standard Loads	Switching Time/r_2C Max	Switching Time/r_2C Min
OR	3	6	1.0	7.4	4.4
AND	2	4	1.3	7.4	5.0
Majority	3	4	1.3	7.4	4.4
AND	3	1.8	1.8	7.4	4.9
Invert	1	5	1.0	7.4	5.5

of the gates have been compiled and extremes in switching time are shown; the effects of variation in diode capacitance, coupling impedances, and transformer loss are not included. A standard load is defined as the input to an OR gate, or 11 per cent I_{max}.

It is possible to simplify loading calculations by adopting a standard load and adjusting the tolerance requirements for each type of gate so that its input requirement is an integral multiple of the standard load.

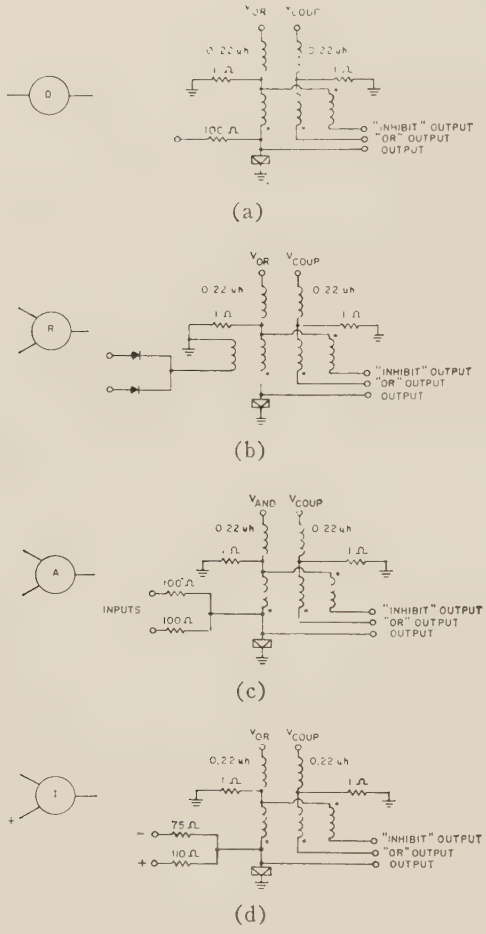

Fig. 19—Experimental monostable circuits. (a) "Delay" gate, (b) OR gate, (c) AND gate, (d) "Inhibit" gate.

For example, the diode tolerance requirements for the OR gate may be relaxed so that its loading is the same as the two-input AND gate and the "Majority" gate. Such a procedure will result in a reduction in logical gain when tolerances are made greater.

Practical Circuits

A set of circuits has been designed using a tunnel diode with a knee current of 20 ma, a nominal capacitance of 200 pf and a negative resistance r_2 of 7 ohms. The resulting nominal switching time was 7.5 nanoseconds and the period of the cycle of operation of the gates was 130 nanoseconds. Figs. 19–21 show several gates with component values. All resistor tolerances are one per cent. The transformers that were used consisted of three primary turns and four secondary turns wound on a General Ceramics type F-303 toroid of *Q*-2 material. The coupling diodes were Transitron type *T*-9.

Acknowledgment

The author wishes to express his appreciation to J. L. Woika for his helpful discussions and assistance.

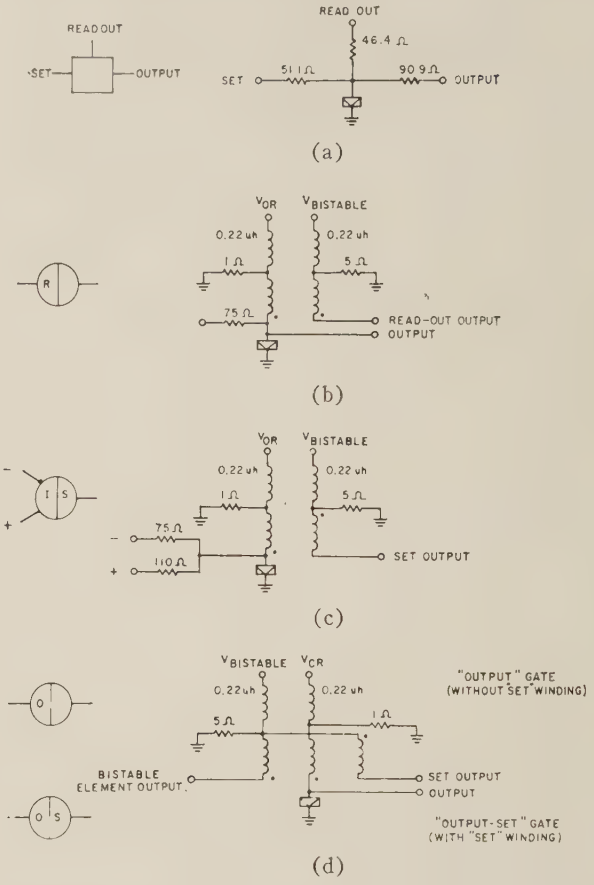

Fig. 20—Experimental bistable circuits. (a) Bistable element, (b) Read-out gate, (c) "Inhibit-set" gate, (d) "Output-set" gate.

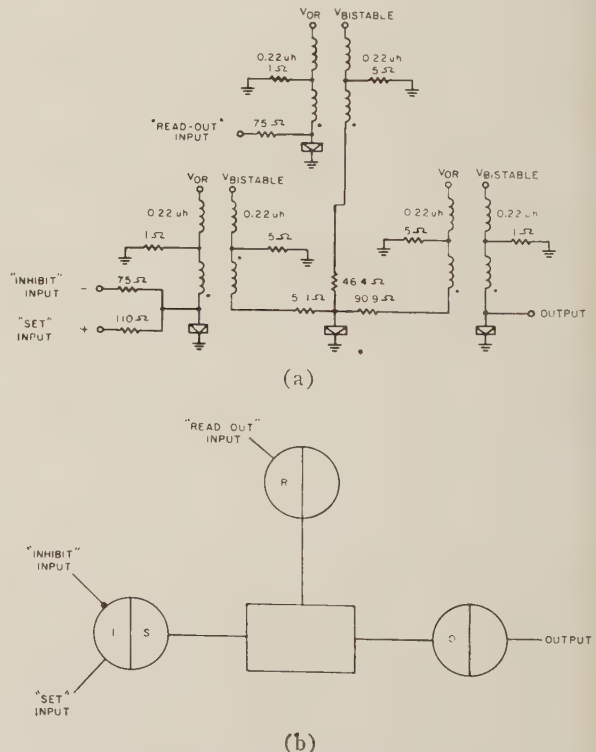

Fig. 21—(a) Circuit diagram of complete storage unit, (b) logi diagram of complete storage unit.

A Secondary-Emission Pulse Circuit, Its Analysis and Application*

JAN A. NARUD†, MEMBER, IRE

Summary—This paper describes a regenerative pulse circuit ing a single secondary-emission tube that is able to generate ılses having a rise time of 6 mμsec and a width continuously variable om 25 mμsec to 12 μsec. First, a theoretical discussion of the circuit given in which expressions for pulse width and rise time are de-ved. Then, various practical realizations of the circuit are presented. mong others, these include a millimicrosecond pulse generator and fast pulse height discriminator.

$$\frac{\dfrac{I_s}{(E_{cs}-E_{co})\cdot C}}{} = \frac{\text{saturation current}}{\text{(grid voltage interval between saturation and cutoff)} \times \text{(total capacitance)}}$$

Introduction

IN the fields of high-speed computers, guided-missile tracking systems, and nuclear physics there has lately been an increasing demand for nonlinear ctive circuits capable of generating pulses in the milli-icrosecond range at high repetition rates. In such cir-uits, thermionic secondary emission tubes show great romise of replacing the ordinary vacuum tube. The easons for this are twofold. First, these tubes have a uch higher ratio between saturation current and elec-ode capacitance than ordinary vacuum tubes, result-ng in a smaller rise time for the same voltage level. econd, with these tubes it is possible to design a posi-ve feedback configuration that has a small loop delay o that the interval between the times it is possible to urn the circuit on and off can be minimized.

This paper describes a regenerative pulse circuit us-ng a single secondary emission tube that is able to gen-rate pulses having a rise time of 6 mμsec and a width ontinuously variable from 25 mμsec to 12 μsec. First, theoretical discussion of the circuit is given in which xpressions for pulse width and resolving time are erived. Then, various practical realizations of the cir-uit are presented. Among others, these include a milli-icrosecond pulse generator and a fast pulse-height dis-riminator.

Besides providing design criteria, the study of the econdary-emission pulse circuit has also served a sec-nd purpose. Since this circuit lends itself so well to nalytical treatment, it has been a great aid in pointing out various general properties of nonlinear circuits of this kind. Among other things, for instance, the analysis suggested that the loop gain was equal to unity at points from which jumps take place. Also, it clearly showed that the figure of merit of how well a vacuum tube will perform in a switching circuit is a ratio of the form

rather than the conventional figure of merit g_m/C.

Description of Secondary Emission Tubes

Although the phenomenon of secondary emission has been used successfully for a long time to amplify the minute photoemission current in photoelectric tubes, its application to thermionic tubes has lagged behind and not until quite recently have reliable tubes of this type become commercially available. Therefore, since they are not yet used universally, a brief discussion will be given of the principles involved.

Fig. 1(a) and 1(b) shows, respectively, the cross section and the circuit symbol of the secondary-emission tube EFP 60 (made by Phillips in Holland). As in a regular pentode, it has a grid and a screen grid, but instead of the suppressor grid it has a pair of focusing electrodes, each consisting of three vertical rods. The secondary-emission electrode, the dynode, practically surrounds the plate, the two parts of which are placed in the two semicylindrical sections of the dynode. After the electrons have been accelerated by the screen, their direction of flow is changed by the focusing electrodes so that the major portion of the electrons strike the cylindrical sections of the dynode. The plate, since it is at a higher potential than the dynode, will attract the secondary electrons emitted from the dynode. To make the plate more susceptible to secondary than to primary electrons, each half is formed as a thin strip with its flat surfaces facing the dynode.

In Fig. 2(a) are shown the plate current, the dynode current, the screen grid current, the cathode current and the grid current as a function of the grid voltage. It is seen that the dynode and the plate current are, respectively, about two and three times that of the cathode current. Also, it should be noted that the grid current is so small compared to the other currents that it may be neglected in the analysis to follow. Finally, in

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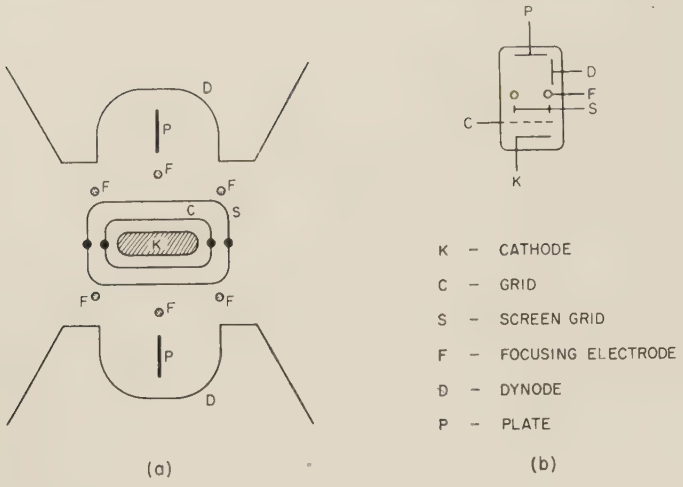


Fig. 1—Cross-section (a) and circuit symbol (b) for the secondary emission tube EFP-60.

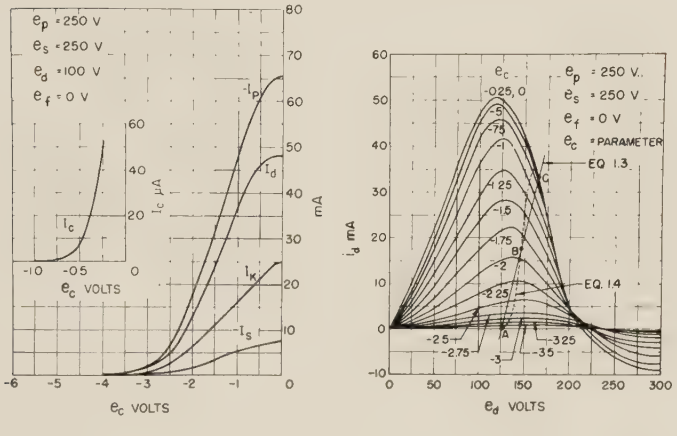


Fig. 2—(a) Plate current (I_p), dynode current (I_d), screen grid current (I_S), cathode current (I_k), and grid current (I_c) as a function of grid-voltage (e_c) for secondary emission tube EFP-60. (b) Dynode-current dynode-voltage characteristics for the secondary emission tube EFP-60.

Fig. 2(b) are shown the current-voltage characteristics of the dynode with the grid voltage as a parameter. It should be noted that the dynode voltage at which maximum secondary emission occurs varies with grid voltage, being about 150 volts for $e_c = -3$ volts and 115 volts for $e_c = 0$ volts.

The Secondary-Emission Pulse Circuit

The circuit diagram of the secondary-emission pulse circuit is depicted in Fig. 3(a). Both the grid and the dynode are coupled to their respective bias supplies E_{cc} and E_{dd} through a resistance and an inductance in series, the inductances being present only for the purpose of compensating for the degenerative effects of the stray capacitances C_d and C_g. The grid and the dynode are coupled together through the capacitor C_c, thereby furnishing a positive feedback loop around these electrodes when the tube is conducting. The trigger source necessary to activate the circuit is represented by the constant current generator coupled to the dynode.

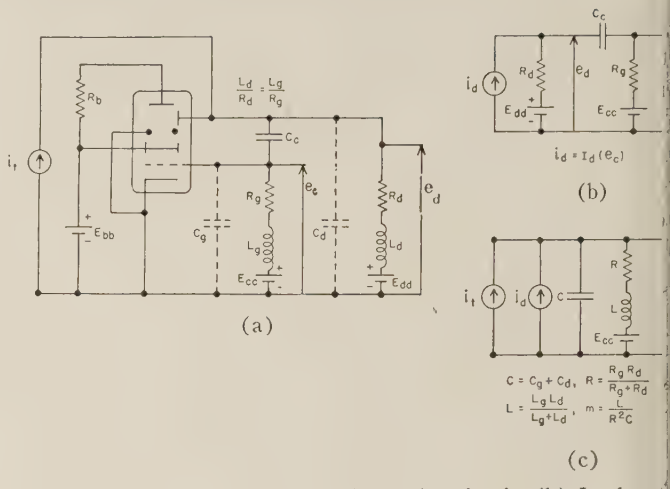


Fig. 3—(a) The secondary emission pulse circuit. (b) Its low-frequency equivalent circuit. (c) Its high-frequency equivalent circuit.

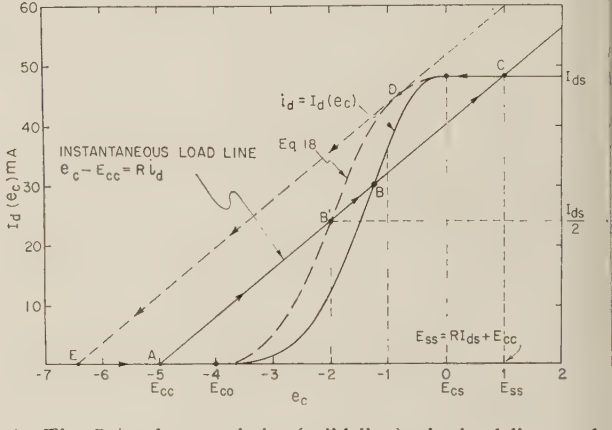


Fig. 4—The I_d/e_c characteristics (solid line), the load line, and approximate tube function (dashed line).

Depending upon the magnitude of the bias volta E_{cc} and the loop gain, the circuit may have a mor stable mode of operation, be free-running, or work as amplifier. We shall first discuss the case in which t circuit is monostable. For such operation, the b E_{cc} must be selected below (or above) the region unity loop gain, and the "instantaneous" load li $e_c - E_{cc} = [(R_g R_d)/(R_g + R_d)]i_d$ should intersect the tu characteristics at three points. This is shown in Fig. where the points A, B and C represent the operati points of the circuit. Since the loop gain is clearly l than one at A and larger than one at B, these are of t stable and unstable kind, respectively. The loop gain C is also less than one, but since the circuit can stay this point only for an instant, this point is quasi-stab

If a trigger signal having sufficient magnitude a duration to drive the circuit past its unstable operati point is applied, the circuit will first flip over to quasi-stable operating point. Then, as the capacitor comes charged, the operating point will move along characteristics until a point is reached at which the lo gain of the circuit becomes equal to unity. This is point D, where the load line is just tangent to the tu

racteristics. A jump now takes the circuit to the nt E, where this load line intersects the e_c axis, after ch the circuit again comes to rest at A.

n analyzing the circuit, we may take advantage of facts that the coupling capacitor C_c is usually much ger than the stray capacitances C_g and C_d, and that series inductances are very small. Therefore, during times the coupling capacitor C_c is charged and dis-rged, the effect of stray capacitances and inductances y be neglected, while when the circuit is triggered l during the jump it may be assumed that the voltage oss C_c stays constant. In other words, the behavior of circuit during the times the tube is conducting and er it has become cut off may be calculated from the ivalent circuit in Fig. 3(b), and its behavior during rapid transitions from the one in Fig. 3(c).

From the equivalent circuit in Fig. 3(b), the equations verning the circuit are:

$$\left(C_c\frac{d}{dt}+\frac{1}{R_g}\right)e_c - C_c\frac{de_d}{dt} = \frac{E_{cc}}{R_g}$$

$$C_c\frac{de_c}{dt}+\left(C_c\frac{d}{dt}+\frac{1}{R_d}\right)e_d = I_d(e_c, e_d)+\frac{E_{dd}}{R_d}. \qquad (1)$$

minating e_d between these two equations we get

$$(R_g + R_d)\frac{de_c}{dt} + \frac{\left[1 - R_d\dfrac{\partial I_d(e_c, e_d)}{\partial e_d}\right](e_c - E_{cc})}{1 - R\left[\dfrac{\partial I_d(e_c, e_d)}{\partial e_c}+\dfrac{\partial I_d(e_c, e_d)}{\partial e_d}\right]} = 0, \qquad (2)$$

ere $R=R_gR_d/R_g+R_d$ and $I_d(e_c, e_d)$ represents the re-ionship of the grid voltage, the dynode voltage and e dynode current given by the tube characteristics. so, the coefficient $C_c(R_g+R_d)$ is the characteristic ne constant of the circuit, and the term

$$\left(1 - R_d\frac{\partial I_d(e_c, e_d)}{\partial e_d}\right)(e_c - E_{cc})$$

presents the steady-state equation; that is, the equa-n governing the circuit during equilibrium. In a operly designed circuit, however,

$$\frac{\partial I_d(e_c, e_d)}{\partial e_d} \neq \frac{1}{R_d},$$

e_c can, at equilibrium, only be equal to E_{cc}. Moreover, the following, the term

$$G = R\left(\frac{\partial I_d(e_c, e_d)}{\partial e_c}+\frac{\partial I_d(e_c, e_d)}{\partial e_d}\right) \qquad (3)$$

ll be defined as the "instantaneous loop-gain function" simply as the loop-gain) of the circuit and, accord-gly,

$$F = 1 - R\left(\frac{\partial I_d(e_c, e_d)}{\partial e_c}+\frac{\partial I_d(e_c, e_d)}{\partial e_d}\right) \qquad (4)$$

is therefore the "instantaneous return difference function." The reasons for defining these quantities in this way are twofold. First, since

$$\frac{\partial I_d(e_c, e_d)}{\partial e_c}$$

represents the transconductance of the tube and

$$-\frac{\partial I_d(e_c, e_d)}{\partial e_d}$$

the dynode conductance, it is evident that G actually represents the loop-gain of the circuit for instantaneous changes of the grid voltage. Second, when the operation of the tube may be regarded as linear, the expressions for G and F reduce to the linear loop-gain and return difference calculated at infinite frequency. To show this, let

$$I_d(e_c, e_d) = I_0 + g_m e_c - g_d e_d, \qquad (5)$$

where g_m and g_d represent the transconductance and dynode conductance of the tube, respectively. Substituting this expression for $I_d(e_c, e_d)$ into (1) and replacing d/dt with the Laplace operator s, the network determinant of the circuit becomes

$$\Delta = \begin{vmatrix} sC_c+\dfrac{1}{R_g}, & -sC_c \\ -(sC_c+g_m), & sC_c+g_d+\dfrac{1}{R_d} \end{vmatrix}, \qquad (6)$$

and therefore the return difference with respect to the tube becomes[1]

$$F(S) = \frac{\Delta}{\Delta_{g_d=0}^{g_m=0}} = 1 - R\,\frac{g_m - g_d\left(1+\dfrac{1}{sC_cR_g}\right)}{1+\dfrac{1}{sC_c(R_g+R_d)}}. \qquad (7)$$

Letting $S\rightarrow\infty$, we have

$$F(\infty) = 1 - R(g_m - g_d) = 1 - R\left(\frac{\partial I_d(e_c, e_d)}{\partial e_c}+\frac{\partial I_d(e_c, e_d)}{\partial e_d}\right) \qquad (8)$$

thus reducing to (4).

As a result of the above discussion, (2) may be written

$$(\text{characteristic time constant})\cdot\frac{d}{dt}(\text{dependent variable}) + \frac{(\text{steady-state equation})}{(\text{instantaneous return difference function})} = 0. \qquad (9)$$

[1] See [1], chs. 4–6, pp. 44–102.

The interesting aspect of this equation is that if we had selected any of the other voltages or currents in the circuit as our dependent variable, the equations obtained would have been exactly of the same form. As a matter of fact, all circuits governed by only one characteristic time constant may be written in the form of (9), and the results arrived at in this paper may therefore be applied to circuits of this kind in general.

Monostable Operation

For the purpose of analyzing the performance of the secondary emission pulse circuit, it is sufficiently accurate to assume that $I_d(e_c, e_d)$ is a function of e_c only. This follows from the fact that when practical embodiments of the circuit are realized, the variation of the dynode voltage is so small that its effect on the dynode current is negligible compared to that of the grid voltage. Thus, (2) may be written:

$$C_c(R_g + R_d)\frac{de_c}{dt} + \frac{e_c - E_{cc}}{1 - R\dfrac{dI_d(e_c)}{de_c}} = 0. \quad (10)$$

Also, under these conditions, the dynode voltage may be explicitly expressed in terms of the grid voltage as follows:

$$e_d = R_d I_d(e_c) - \frac{R_d}{R_g}(e_c - E_{cc}) + E_{dd}. \quad (11)$$

From (10) it is seen that the slope of the time response, de_c/dt, is infinite when the loop-gain,

$$G = R\frac{dI_d(e_c)}{de_c}, \quad (12)$$

becomes equal to unity, thus indicating that a jump may take place from such a point. Accordingly, the values of the grid voltage, e_{cj}^-, that represent jump points may be found by equating the loop-gain function equal to unity:

$$R\frac{dI_d(e_c)}{de_c}\bigg|_{e_c=e_{cj}} = 1. \quad (13)$$

The voltage attained by the grid after the jump is found from the fact that the energy stored in the system cannot change instantaneously. Thus, the voltage across the coupling capacitor must stay constant during the jump, which allows us to write

$$e_{dj}^- - e_{cj}^- = e_{dj}^+ - e_{cj}^+, \quad (14)$$

where (e_{cj}^-, e_{dj}^-) and (e_{cj}^+, e_{dj}^+) represent respectively the voltages at the grid and the dynode before and after the jump. Substituting for e_{dj}^- and e_{dj}^+ from (11), (14) may be written:[2]

$$e_{cj}^+ - RI_d(e_{cj}^+) = e_{cj}^- - RI_d(e_{cj}^-). \quad (15)$$

[2] It should be noted that if E_{cc} is substituted for e_{cj}^- and e_c for e_{cj}^+, this equation reduces to the equation for the instantaneous load line in Fig. 4; that is, $e_c - E_{cc} = RI_d(e_c)$.

When the circuit has a monostable mode of operatic however, the tube is cut off after the jump; *i.* $I_d(e_{cj}^+) = 0$, and the final form of (15) becomes

$$e_{cj}^+ = e_{cj}^- - RI_d(e_{cj}^-). \quad (1$$

To solve (10), we must obtain an analytical expressi for the tube characteristics. In this paper, we will a proximate the characteristics with a function that zero below cutoff, $e_c \leq E_{co}$, equal to I_{ds} above the satu tion point, $e_c \geq E_{cs}$, and represented by a ratio of t second-degree polynomials in the interval $E_{co} \leq e_c \leq E$

$$I_d(e_c) = \frac{N_2 e_c^2 + N_1 e_c + N_o}{e_c^2 + D_1 e_c + D_o}. \quad (1$$

The five coefficients of these two polynomials can be d termined by requiring that the value of (17) and slope shall be the same as the actual tube charact istics at a prescribed number of points. Specifying, f instance, that (17) shall go through the points

$$(E_{co}, 0), \left(\frac{E_{cs} + E_{co}}{2}, \frac{I_{ds}}{2}\right) \text{ and } (0, I_{ds})$$

and requiring the slope to be equal to zero at the fi and last of these points, we have enough information determine all of the coefficients. Thus, the resulting e pression for $I_d(e_c)$, becomes

$$I_d(e_c) = I_{ds}, \qquad e_c \geq E_{cs} \quad (18$$

$$I_d(e_c) = \frac{I_{ds}}{2}\frac{(e_c - E_{co})^2}{\left(\dfrac{E_{cs} - E_{co}}{2}\right)^2 + \left(e_c - \dfrac{E_{cs} + E_{co}}{2}\right)^2},$$

$$E_{co} \leq e_c \leq E_{cs} \quad (18$$

$$I_d(e_c) = 0, \qquad e_c \leq E_{co}. \quad (18$$

The dashed curve in Fig. 4 shows a plot of this functio It is seen that it resembles quite closely the behavior the tube characteristics, and it is therefore to be e pected that the solution of (10), with this function su stituted for the real $I_d(e_c)$, should approximate the exa behavior of the circuit very closely. Indeed, experimen bear this out.

The solution to (10) is greatly simplified if the ind pendent and dependent variables are normalized. Thu if we substitute for t and e_c

$$t = \tau(R_g + R_d)C_c \quad (1$$

$$e_c = \frac{E_{cs} - E_{co}}{2}x + \frac{E_{cs} + E_{co}}{2}, \quad (2$$

which define τ and x, and call

$$I_d(e_c) = \frac{I_{ds}}{2}f(x), \quad (2$$

$$y = 2\frac{e_d - E_{dd}}{E_{cs} - E_{co}}, \quad (2$$

$$\alpha = 1 + 2\frac{E_{co} - E_{cc}}{E_{cs} - E_{co}}, \tag{23}$$

$$\beta = \frac{RI_{ds}}{E_{cs} - E_{co}}, \tag{24}$$

$$\gamma = 1 + \frac{R_d}{R_g}, \tag{25}$$

en (10), (11), (13), (16) and (18) become, respectively:

$$\frac{dx}{d\tau} + \frac{x + \alpha}{1 - \beta\dfrac{df(x)}{dx}} = 0, \tag{26}$$

$$y = \beta\gamma f(x) - (\gamma - 1)(x + \alpha), \tag{27}$$

$$\beta \cdot \frac{df(x)}{dx}\bigg|_{x=x_j^-} = 1, \tag{28}$$

$$x_j^+ = x_j^- - \beta f(x_j^-), \tag{29}$$

$$f(x) = 2, \qquad x \geq 1 \tag{30a}$$

$$f(x) = \frac{(x+1)^2}{x^2+1}, \qquad -1 \leq x \leq 1 \tag{30b}$$

$$f(x) = 0, \qquad x \leq -1. \tag{30c}$$

these equations, x, y and $f(x)$ represent the normal-
d grid voltage, dynode voltage, and tube function,
pectively. The cutoff point, E_{co}, is now located at
$= -1$ and the saturation point, E_{cs}, at $x = 1$. The pa-
meter α represents the normalized grid bias and β the
responding normalized value of load resistance R.
e normalized saturation current is equal to 2 and the
rmalized loop-gain of the circuit is $\beta[df(x)/dx]$.
ally, the stable (A) and the quasi-stable (C) operat-
points are located at $-\alpha$ and $2\beta - \alpha$, respectively.
The general solution of (26) is of the form

$$\tau - \tau_o = \beta \int \frac{df(x)}{x + \alpha} dx - \ln(x + \alpha) \tag{31}$$

$$- \tau_o = \beta\left(\frac{f(x)}{x+\alpha} + \int \frac{f(x)}{(x+\alpha)^2} dx\right) - \ln(x + \alpha), \tag{32}$$

ere τ_o is a constant of integration. Substituting suc-
sively the expressions for the normalized tube func-
n $f(x)$ into these equations, specifying that the initial
ue of x is $2\beta - \alpha$ and matching the boundary condi-
ns between the three intervals, we get these respective
utions of (26):

$$\tau = \ln \frac{2\beta}{x + \alpha} \tag{33a}$$

when $x \geq 1$;

$$\tau = \frac{2\beta}{(\alpha^2+1)^2}\left[(\alpha^2+1)\left(\frac{\alpha x + 1}{x^2+1} - \frac{\alpha+1}{2}\right) + 2\alpha\left(\arctan x - \frac{\pi}{4}\right) + \frac{\alpha^2 - 1}{2}\ln\frac{(1+\alpha)^2(x^2+1)}{2(x+\alpha)^2} + \ln\frac{2\beta}{x+\alpha}\right], \tag{33b}$$

when $-1 \leq x \leq 1$; and

$$\tau = \ln \frac{x_j^+ + \alpha}{x + \alpha} + \tau_W \tag{33c}$$

when $x \leq -1$.

In the last equation, τ_W is the time when the jump takes place, or in other words, the value attained by (33b) when x becomes equal to x_j^-. The quantity x_j^+ represents the normalized grid voltage at the end of the jump and is given by (29).

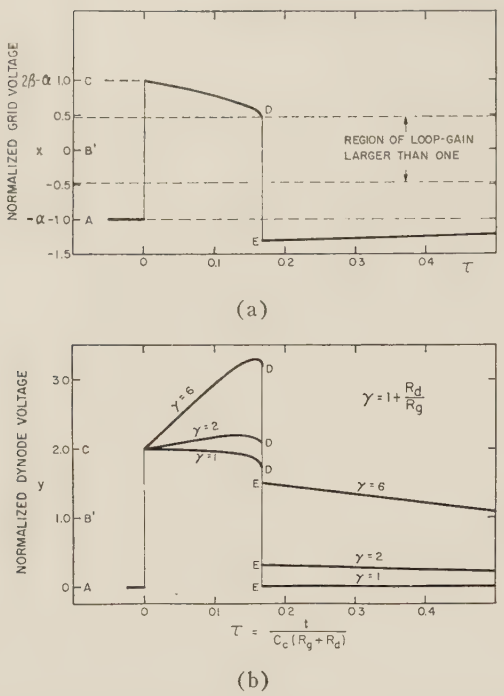
In terms of these equations, if the circuit is initially resting at the stable operating point ($x = -\alpha$) and a trigger signal of sufficient width and magnitude is applied, the circuit will first jump over to its quasi-stable operating point located at $x = 2\beta - \alpha$. The grid voltage will then start to decay according to (33a) until the saturation point, $x = 1$, is reached, after which it will proceed in conformance with (33b). This equation, in turn, will govern the response up to the time the loop gain of the circuit becomes equal to unity; *i.e.*, when $x = x_j^-$. Substituting for $f(x)$ in (28), we can express the location of this point explicitly in terms of β, as

$$x_j^- = \sqrt{\sqrt{\beta(\beta+4)} - (1+\beta)}. \tag{34}$$

As explained before, at the unity loop-gain point, a jump takes place to the point x_j^+, given by (29), after which the stable operating point is approached exponentially according to (33c).

It should be noted that, according to (34), actually two points of unity loop gain exist. The other one, corresponding to a minus sign in front of the outer square root, is located between the stable and the unstable operating points, and jumps therefore cannot take place from it. However, if both the operating points A and C had been of the quasi-stable kind, jumps would have taken place from both of the unity loop-gain points.

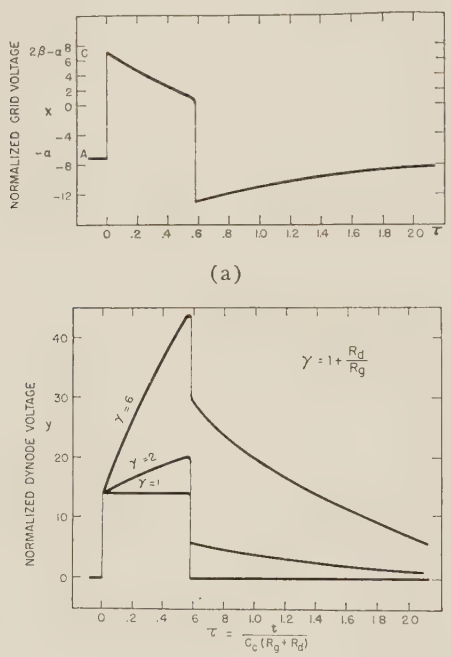
The results of calculating the grid voltage response from these equations are shown in Figs. 5(a), 6(a), and 7(a). Also depicted together with these are the corresponding dynode voltages as calculated from (27). In the first of these figures, $\alpha = \beta = 1$, which represents the case where the stable operating point is located at the cutoff point, E_{co}, in Fig. 4 and the quasi-stable one at the saturation point, E_{cs}; *i.e.*, the points at which the tube has just barely become cutoff and saturated. Since it is important to make the circuit relatively independent of changes in the tube characteristics, deviations



(a)

(b)

Fig. 5—(a) Calculated transient response of the grid voltage. (b) Transient response of the dynode voltage for various values of γ.

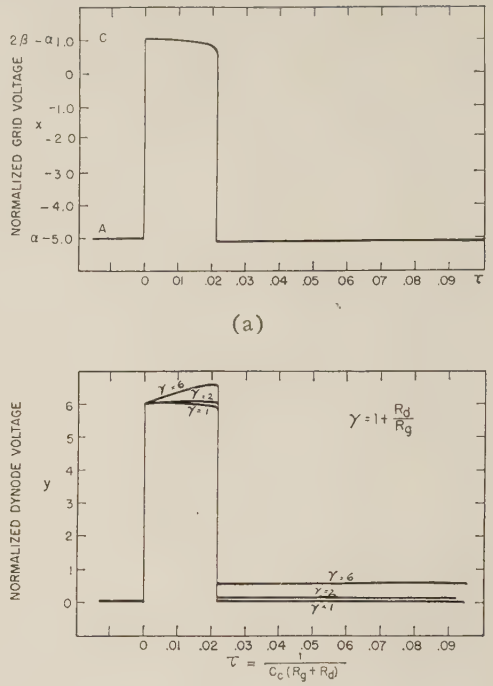


(a)

(b)

Fig. 6—Calculated responses (a) of the grid voltage and (b) of the dynode voltage for various values of α, when $\alpha = \beta = 7$.

from the nominal value of circuit components, spurious trigger signals, noise, etc., the bias E_{cc} should not be selected larger than E_{co} and the slope of the load line in Fig. 4 not less than that of the line going through the cutoff and the saturation points. Hence, the case depicted in Fig. 5 may be regarded as the case where the parameters α and β attain their minimum values. Fig. 6(a) shows the effect of increasing both α and β to seven, which on the i_d/e_c characteristics is equivalent to moving



(a)

(b)

Fig. 7—Calculated responses (a) of the grid voltage and (b) of t dynode voltage for various values of α, when $\alpha = 5$, and $\beta = 3$.

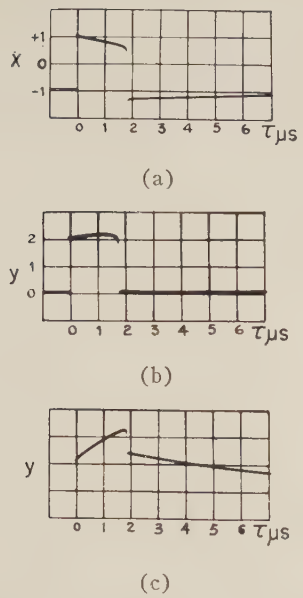
the stable operating point $3(E_{cs} - E_{co})$ units to the le of E_{co} and the quasi-stable point to the right of E_{cs} b the same amount. It is seen that both the pulse widt and the undershoot have now increased considerabl being now roughly three times as large as in the previo case. Moreover, in Fig. 7(a) is shown the consequence increasing α and β in such a way that the stable opera ing point moves beyond E_{co} while the quasi-stable poi remains fixed at E_{cs}; *i.e.*, $2\beta - \alpha = 1$. Rather than beir increased, the pulse width and the undershoot have no decreased about nine times. Also, the grid voltage pul is now squarer in shape. Finally, from the responses the dynode voltage it should be noted that the oversho of this voltage just after the jump has the same ma nitude as the corresponding undershoot of the grid vol age when $\gamma = 2$.

These results agree very well with experimentally o tained responses as can be seen from Fig. 8, which di plays oscillographic pictures of the grid and the dyno voltages for the case when $\alpha = \beta = 1$. For instance, bo calculations and measurements show the pulse width be slightly less than $0.2(R_g + R_d)C_s$ and the undersho of the grid voltage about 15 per cent.

The normalized pulse width for any value of α and can be found from (33b) by substituting x_j^- for x in it. However, since the quantity x_j^- is only a functi of β, the expression for the absolute pulse width may written as

$$T_W = (R_g + R_d)C_c\tau_W(\alpha, \beta), \qquad (3$$

where $\tau_W(\alpha, \beta)$ represents (33b) when $x = x_j^-$. Solvi for R_g and R_d from (24) and (25) and substituting f



g. 8—$C_c(R_g+R_d)=10$ μsec scale: 1 μsec/division. Transient response (a) of the grid voltage; (b) of the dynode voltage, with $\gamma=2$; and (c) of the dynode voltage, with $\gamma=6$.

ese two quantities, we may also write the above uation as:

$$T_W = \frac{\gamma^2}{\gamma-1}\,\frac{E_{cs}-E_{co}}{I_{ds}}\,C_c\beta\tau_W(\alpha,\beta). \tag{36}$$

Fig. 9 are shown the variations of the normalized lse width, $\tau_W(\alpha, \beta)$, for various values of α and β. It seen also that this figure suggests that the pulse dth normally increases with β unless $2\beta-\alpha=1$, in hich case it decreases. That this is true in general for e normalized as well as the absolute pulse width can seen by taking the limit of (36) as α and β become rge. It is easily shown from (34) that x_j^- approaches and from (33b) that

$$T_W \to \frac{\gamma^2}{\gamma-1}\,\frac{E_{cs}-E_{co}}{I_{ds}}\,C_c \ln\left(\frac{2\beta}{x_j^- + \alpha}\right)^{\beta} \tag{37}$$

r large α and β. Hence, the absolute pulse width will crease with β as long as $2\beta-\alpha>1$, but decrease to zero nen $2\beta-\alpha=1$. Also, it is evident that the change of lse width for a given variation of β is greater as $2\beta-\alpha$ comes larger, that is, the further away from the satution point the quasi-stable operating point is located. For all practical purposes it is sufficiently accurate to glect the terms within the large parentheses of (33b) nen the pulse width is calculated. Thus, the expression r the absolute pulse width reduces to

$$T_W \approx (R_g + R_d)C_c \ln\frac{2\beta}{x_j^- + \alpha}, \tag{38}$$

$$T_W = \frac{\gamma^2}{\gamma-1}\,\frac{E_{cs}-E_{co}}{I_{ds}}\,C_c\beta \ln\frac{2\beta}{x_j^- + \alpha}, \tag{39}$$

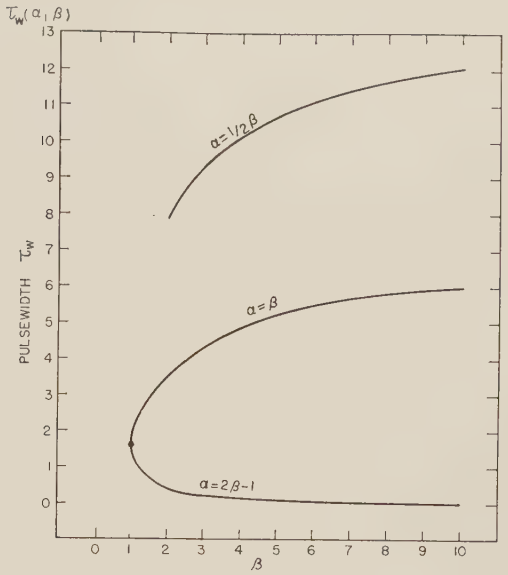


Fig. 9—The normalized pulse width as a function of α and β.

where x_j^- is, as before, given by (34). From (35) and (38), it is seen that the absolute pulse width is linearly proportional to C_c but only approximately so to R_g (or R_d) when $\gamma\sim1$. The latter statement follows from the facts that when $\gamma\sim1$, $R_d\ll R_g$, $R\sim R_d$ and therefore independent of R_g. Also, it should be noted that the minimum value of the term $\gamma^2/\gamma-1$ occurs when $\gamma=2$. Hence, when the time consumed by the fast transitions may be neglected, minimum pulse width is obtained if $R_g=R_d$, $2\beta-\alpha=1$ and if α and β are chosen as large as possible. In such cases the pulse width is approximately

$$T_{W\min} \approx 4\,\frac{E_{cs}-E_{co}}{I_{ds}}\,C_c\beta \ln\frac{2\beta}{1+\alpha}. \tag{40}$$

When the circuit must operate with a high duty-factor, it is important to make the undershoot (or the overshoot) and the recovery time as small as possible. Therefore, it is worthwhile to investigate how these quantities may be minimized. The fractional undershoot of the grid voltage in units of the initial pulse height, 2β, may, from (29), be written as:

$$\rho = \frac{-\alpha - x_j^+}{2\beta} = \frac{\beta(f(x_j^-)) - (x_j^- + \alpha)}{2\beta}. \tag{41}$$

Introducing the fact that for dependable operation the quasi-stable operating point should be located at or above the saturation point; that is, $2\beta-\alpha\geq1$, the above equation becomes:

$$\rho \geq \frac{1-x_j^-}{2\beta} + \frac{f(x_j^-)}{2} - 1. \tag{42}$$

Hence, the undershoot is smallest when $2\beta-\alpha=1$; *i.e.*, when the quasi-stable operating point is located at E_{cs}. Also, since x_j^- increases monotonically from 0.486 to 1 when β is varied from its minimum value of 1 to infinity, α and β should also be selected as large as possible.

Furthermore, the time it takes the grid voltage to recover from the value it has just after the jump to a certain prescribed interval, ϵ, away from the stable operating point, may be found from (33c) by substituting $-\alpha-\epsilon$ for x into it. Thus,

$$T_R = (R_g + R_d)C_c \ln \frac{\beta f(x_j^-) - (x_j^- + \alpha)}{\epsilon}, \qquad (43)$$

where we have introduced the expression for x_j^+ from (29). Substituting, as before, for R_g and R_d from (24) and (25), we may also write this equation as

$$T_R = \frac{\gamma^2}{\gamma - 1} \frac{E_{cs} - E_{co}}{I_{ds}} C_s \ln \frac{\beta f(x_j^-) - (x_j^- + \alpha)}{\epsilon}. \qquad (44)$$

Introducing again the fact that $2\beta-\alpha \geq 1$, it is easily shown also that T_R will be smallest when $2\beta-\alpha=1$ and when α and β are chosen as large as possible. Also, by differentiating the term $\gamma^2/\gamma-1$ it is found that it is minimum when $\gamma=2$. Moreover, from (27) it can be seen that the recovery of the dynode voltage is equal to or faster than that of the grid voltage when $\gamma=2$; so the above conditions are also compatible with the recovery of the dynode voltage as well. Hence, when the circuit must operate under high duty-factor conditions, the quasi-stable operating point should be located at the point of saturation, α and β should be selected large, and R_g should be made equal to R_d. Also, if it is desirable to vary the pulse width, by the same token this should be done by changing C_c rather than R_g or R_d.

It should be pointed out, however, that these conditions are somewhat modified when the pulse width is small and the repetition rate high, since the effect of the stray capacitances and the trigger signal must then be taken into account. This, as we shall see later, requires that α and β be selected close to unity.

Astable Operation

If the bias voltage E_{cc} is chosen within the region of loop gain larger than one, the operating point at A will also be of the quasi-stable kind. In other words, the unstable operating point is now located between two semi-stable operating points, and jumps may therefore take place from each of the unity loop-gain points. Thus, a limit cycle may be formed around the unstable operating point and sustained relaxation oscillations result.

The basic equations governing these oscillations are the same as those controlling the transient response in the monostable case. The only changes are that now the solutions to (32) have to be applied repeatedly over the cycle and that the boundary conditions between the intervals, in which these equations are valid, are different. Referring to Fig. 10 for the significance of the various symbols, we see that the equations governing the response of the normalized grid voltage in this case are

$$\tau = \ln \frac{x_{j-1}^+ + \alpha}{x + \alpha} + \tau_{j-1}, \qquad (45)$$

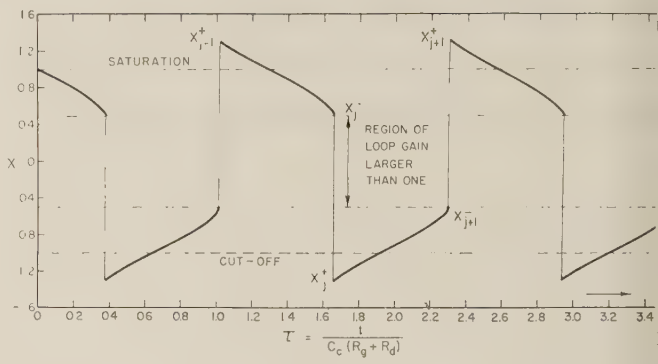


Fig. 10—Response of the grid voltage when the circuit is astal

for $1 \leq x \leq x_{j-1}^+$, and

$$\tau = \frac{2\beta}{(\alpha^2+1)^2}\left\{(\alpha^2+1)\left(\frac{\alpha x+1}{x^2+1} - \frac{\alpha+1}{2}\right) + 2\alpha\left(\arctan x - \frac{\pi}{4}\right) + \frac{\alpha^2-1}{2}\ln\frac{(x^2+1)(1+\alpha)^2}{2(x+\alpha)^2}\right\} + \ln\frac{x_{j-1}^+ + \alpha}{x+\alpha} + \tau_{j-1}$$

in the interval $1 \geq x \geq x_j^- = \sqrt{\sqrt{\beta(\beta+4)} - (1+\beta)}$.

As before, when the unity loop-gain point x_j^- is reached, a jump takes place to the point

$$x_j^+ = x_j^- - f(x_j^-),$$

after which

$$\tau = \ln \frac{x_j^+ + \alpha}{x+\alpha} + \tau_j$$

when $x_j^+ \leq x \leq -1$ and

$$\tau = \frac{2\beta}{(\alpha^2+1)^2}\left\{(\alpha^2+1)\left(\frac{\alpha x+1}{x^2+1} - \frac{1-\alpha}{2}\right) + 2\alpha\left(\operatorname{arctg} x + \frac{\pi}{4}\right) + \frac{\alpha^2-1}{2}\ln\frac{(x^2+1)(\alpha-1)^2}{2(x+\alpha)^2}\right\} + \ln\frac{x_j^+ + \alpha}{x+\alpha} + \tau_j$$

for

$$-1 \leq x \leq x_{j+1} = -\sqrt{\sqrt{\beta(\beta+4)} - (1+\beta)}.$$

When x attains the value, x_{j+1}^-, of the other loop-g point, a jump again takes place. However, this time is in the upward direction to a point beyond the se stable operating point C, given by:

$$x_{j+1}^+ = x_{j+1}^- + \beta(2 - f(x_{j+1}^-)).$$

After this jump the cycle is completed and the respons again governed by (45). Also, from (49) and (46), it c easily be shown that the period of the oscillations

pproximately given by

$$T_p \approx (R_g + R_d)C_c \ln \frac{x_j^+ + \alpha}{x_{j+1}^- + \alpha} \cdot \frac{x_{j+1}^+ + \alpha}{x_j^- + \alpha}$$

$$\approx \frac{\gamma^2}{\gamma - 1} \frac{E_{cs} - E_{co}}{I_{ds}} C_c \beta \ln \left(1 - \frac{2\beta}{\alpha + x_j^-}\right) \cdot \left(1 + \frac{2\beta}{\alpha - x_j^-}\right). \quad (51)$$

rom this expression, it is easily shown that the period a minimum when $\alpha = \beta = 1$ and when $\gamma = 2$. This is the ase shown in Fig. 10.

Finally, if E_{cc} is selected within the conducting region f the tube and if the loop-gain is less than one, the cir- uit of Fig. 3 operates as an amplifier. Because of the ositive feedback, it can be made very sensitive. This, ombined with the fact that these tubes saturate easily, nakes such an amplifier ideal as a trigger source. Also, y selecting $g_m \cdot R_d > 1$ it is possible to cancel out some f the circuit capacity by the negative capacitance in- roduced by the positive feedback.

Calculation of Rise Time and Minimum Pulse Width

In order to obtain a reasonably accurate estimate of he rise time and the minimum pulse width obtainable rom the circuit, we must consider the effects of stray apacitances, series inductances and the trigger signal. However, the coupling capacitor C_c may be neglected ince it is usually much larger than the grid-to-ground apacity. Thus, we obtain the equivalent circuit of Fig. (c), from which the differential equation governing the rid voltage during the rapid transitions becomes

$$LC \frac{d^2 e_c}{dt^2} + \left[RC - L \frac{dI_d(e_c)}{de_c}\right] \frac{de_c}{dt} + e_c - E_{cc} = RI_d(e_c) + \left(R + L \frac{d}{dt}\right) I_t(t), \quad (52)$$

where $I_t(t)$ represents the current delivered to the circuit by the trigger source. The equation obtained by setting $I_t(t)$ and the derivatives of e_c equal to zero,

$$e_c - E_{cc} = RI_d(e_c), \quad (53)$$

epresents the equation that determines the operating oints the circuit may temporarily have during the ransitions. In other words, it is the equation governing he "instantaneous" load line in Fig. 4. Normalizing, as efore, the dependent variable according to (20) but hanging the normalization of time to

$$\tau = \frac{t}{RC} \quad (54)$$

nd calling

$$m = \frac{L}{R^2 C}, \quad (55)$$

$$I_t(t) = \frac{I_{ds}}{2} g(\tau), \quad (56)$$

we see that (52) and (53) become, respectively:

$$m \frac{dx^2}{d\tau^2} + \left(1 - m\beta \frac{df(x)}{dx}\right) \frac{dx}{d\tau} + x + \alpha = \beta f(x) + \left(1 + m \frac{d}{d\tau}\right) g(\tau) \quad (57)$$

and

$$x + \alpha = \beta f(x). \quad (58)$$

In general, the delay and rise time of the circuit are proportional to the effective load resistance R, and in order to make the transitions as rapid as possible R should be selected as small as possible. On the other hand, the demand for dependable operations requires that R should not be selected smaller than the value that causes the stable operating point to be located at cutoff (E_{co}) and the semistable one at the saturation point (E_{cs}). Hence, in order to investigate what the optimum switching conditions are, we need only consider the case when $\alpha = \beta = 1$, and (57) may be written

$$m \frac{dx^2}{d\tau^2} + \left(1 - m \frac{df(x)}{dx}\right) \frac{dx}{d\tau} + x + 1 = f(x) + \left(1 + m \frac{d}{d\tau}\right) g(\tau). \quad (59)$$

As representative of typical trigger signals, the function $g(\tau)$ will in the following be assumed to be in the form of a ramp function pulse as shown in Fig. 11. The

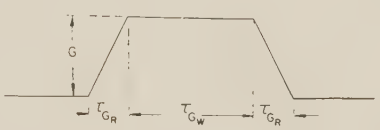


Fig. 11—Assumed trigger function, normalization: $\tau = t/RC$.

results of solving (59) numerically for various values of the rise τ_{GR}, width τ_{GW}, and magnitude G of this trigger function are shown in Figs. 12 and 13. The calculations, were carried out for two values of m, namely, $m = 0$ and $m = 0.5$. In both cases, it was assumed that the circuit was initially at rest at the stable operating point at $x = -1$ and that $x'(0+) = 0$. Corresponding values of τ_{GR}, τ_{GW} and G of each curve are given in Table I, in which the normalized delay, rise and resolving times of each response are also listed. The resolving time, τ_S, is here defined as the time it takes the response to traverse 90 per cent of the interval between its initial and maximum values. The advantage of this definition is that it partially takes into account the hampering effects of large delays and overshoots.

The significance of the different transient responses in Figs. 12 and 13 can be summarized as follows: The

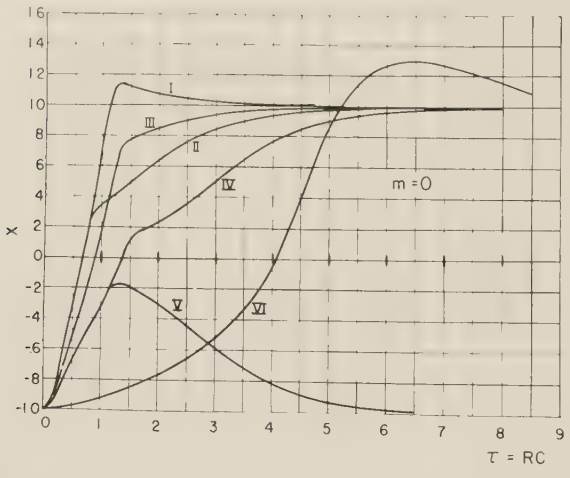


Fig. 12—Transient responses of the circuit in Fig. 3(c) to different types of trigger signals when $m=0$.

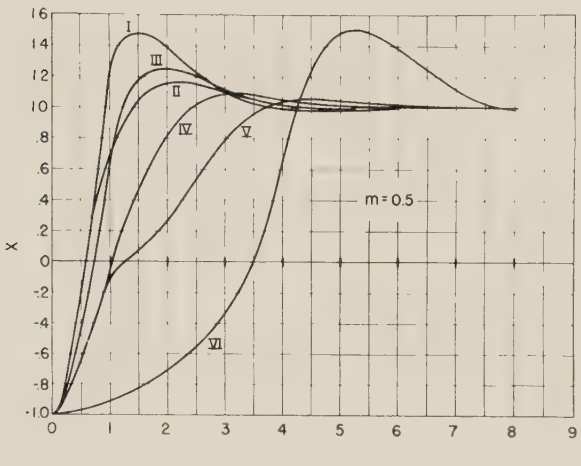


Fig. 13—Transient responses of the circuit in Fig. 3(c) to different types of trigger signals when $m=0.5$.

TABLE I

NORMALIZATION: $\tau=t/RC$

No.	m	G	τ_{GR}	τ_{GW}	τ_D Delay	τ_R Rise	τ_S Resolution
I	0	2	0.25	0.85	0.7	0.8	1.1
II		2	0.25	0.45	0.7	2.5	2.7
III		1.5	0.25	0.95	0.9	1.35	1.65
IV		1	0.25	1.15	1.4	3.8	4.2
V		1	0.25	0.85	—	—	—
VI		0.816	4.08	0	4.1	3.1	5.35
I	0.5	2	0.25	0.64	0.6	0.6	1
II		2	0.25	0.35	0.6	0.9	1.35
III		1.5	0.25	0.71	0.75	0.85	1.25
IV		1	0.25	0.81	1.05	1.65	2.1
V		1	0.25	0.61	1.25	2.7	3.15
VI		0.7	3.5	0	3.5	2.55	4.5

two curves labeled I represent the transient responses when the applied trigger signal has a normalized magnitude of 2 and a rise time of 0.25. The width τ_{GW} was adjusted such that the trigger function started to decay when x reached the value 0.9. Comparing the two curves, we see that the resolving times equal 1.1 and 1.0, respectively, and that the curve in Fig. 13 has conside ably more overshoot. Also, it should be noted that, sinc the trigger current is here equal to the saturation curre of the tube, these cases represent the conditions und which the respective resolving times are minimized.

In the second case (II), the width of the trigger fun tion was adjusted in such a manner that it started decay when x was equal to zero, while the magnitud and rise of the former case were retained. It can be see that the resolving times have now increased conside ably, to 2.7 and 13.5, respectively. For dependab transition from the stable to the semistable operatin points, trigger signals having less pulse width than i dicated here should not be used.

The third case (III) illustrates the effect of reducin both the magnitude and the width of the trigger fun tion, which was now made to decay when the transie responses reached $x=0.5$. Comparing the values of th resolving times here with those of case I, it can be see that they have increased only slightly.

In cases IV and V, the responses of small and narro trigger signals are considered. In the former case, th trigger started to decay at $x=0$; and in the latter, $x=-0.25$. From Table I it is seen that the resolvin time with $m=0$ has now increased nearly four times ov that of case I, while the corresponding factor for th shunt-peaked circuit is only 2.1. In case V, the trigg signal did not have sufficient magnitude and duratic to make the circuit register it when $m=0$. In the shun peaked circuit, however, enough energy was stored i the inductance by the trigger source to slide the circu past the unstable operating point ($x=0$).

Finally, the effect of a trigger signal with a slow ris time is illustrated (VI). The trigger function was a sumed to rise with a slope of 0.2 until the correspondin transient responses reached zero, at which time it wa made to decay with the same slope. It is seen fro Table I that not only are the resolving times ver large in this case, but also only a slight improvemer is obtained by using a shunt-peaked circuit.

From the above considerations, it is evident that th transient response of a circuit of this type is greatly a fected by the magnitude and shape of the applied trigg signal. Depending upon the characteristics of this fun tion, values of the normalized resolving time rangin from about 1.0 to 5.5 may be obtained. Ideally, th applied trigger pulse should have a magnitude as larg as possible and a width sufficient to drive the circuit t 50–80 per cent of the interval past its unstable operatin point ($x=0.5\rightarrow0.8$).

Comparing the transient responses in Figs. 12 and 1 it can be seen that the curves have more overshoot an do not change so abruptly in the shunt-peaked cas This is, of course, due to the energy stored in th inductance-supplying current to the circuit after th trigger signal has vanished. Also, it is evident fro Table I that the improvement obtained by using shunt-peaked circuit is much greater for trigger pulse

aving smaller magnitudes and widths than for those ith larger ones: in cases II and IV, for example, the solving times are one half as large as those obtained hen $m = 0$, while in case I the improvement is only 0.91. n other words, shunt-peaking has the effect of making ie circuit more independent of the shape and magnide of the trigger signal.

The minimum pulse width obtainable from the circuit Fig. 3(a) can also be estimated from these curves. If fast trigger signal is applied, the circuit will turn on ore or less as indicated by curve I or II in Fig. 13. loreover, the approximate time taken for the circuit to mp from the unity loop-gain point to the stable opering point may be found by regarding the charging curnt to the coupling capacitor C_c as a slow trigger signal ith small magnitude. Hence, one should expect the reponse of the jump to resemble a curve located somehere in between curves IV and VI. Thus, by computing ie times elapsed between the 50 per cent levels of urves I and IV, and of curves II and VI, when it is ssumed that IV and VI start at the maximum point of urves I and II, respectively, the lower and upper limits f the minimum pulse width (50 per cent width) become:

$$T_{W\min} = (2 \rightarrow 5.2)\frac{E_{cs} - E_{co}}{I_{ds}}C = (2 \rightarrow 5.2)\frac{R_d \cdot R_g}{R_d + R_g}C. \qquad (60)$$

or the circuit in Fig. 3(a), the total capacitance of ynode, grid and stray is about 30 $\mu\mu$f, and the expected inimum pulse width should therefore lie in the range 5 to 37 mμsec. This is in excellent agreement with exeriment, which showed the minimum pulse width to e about 25 mμsec. Finally, it should be noted that the esolving time and the minimum obtainable pulse width re inversely proportional to the ratio

$$\eta = \frac{I_{ds}}{(E_{cs} - E_{co})C} = \frac{\text{saturation current}}{\text{(voltage interval between saturation and cutoff) (total capacitance)}}. \qquad (61)$$

Hence, this ratio may be regarded as a figure of merit ndicating how well a certain tube will perform in a vitching circuit, in much the same manner that the atio g_m/C indicates its applicability as a wide-band mplifier. Since the possibility exists in secondary-emison tubes of increasing their saturation current without n appreciable increase of capacitance, these tubes ossess a great potentiality in high-speed pulse circuits.

Practical Circuits

Fig. 14 shows a practical version of the secondaryission pulse circuit. The tube T_2 and its associated rcuit constitute the regenerative part of the pulse cirit, and T_1 serves as a trigger amplifier. Both tubes are ormally biased to cutoff. The plate of the trigger tube coupled to the cathode of T_2 through a capacitor so

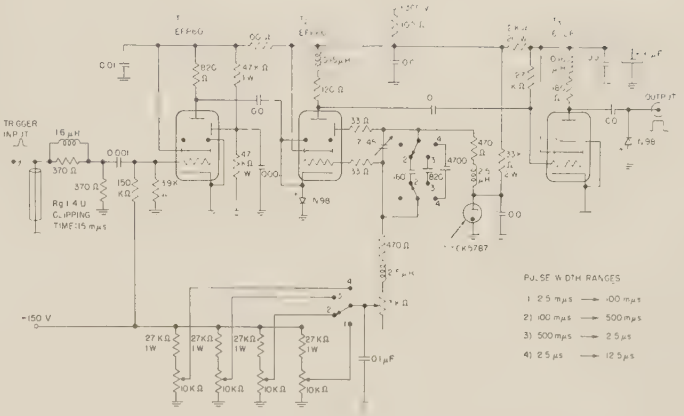


Fig. 14—A practical version of the secondary emission pulse circuit. (*Note:* Capacitance values less than 1 in μf and above 1 in $\mu\mu$f, unless otherwise noted.)

that when a positive trigger signal is applied to the grid of T_1, the cathode of T_2 goes negative, setting off the regenerative action of the circuit. The purpose of the diode between the cathode of T_2 and ground is to make the cathode impedance large during the duration of the trigger signal but small when T_2 becomes conducting. In this way, practically all of the plate current of the trigger tube is used to turn T_2 on, thereby assuring rapid and precise trigger action. Moreover, to prevent trigger signals having a long tail from retriggering the circuit when the regenerative action is completed, a short-circuited coaxial cable is connected across the input.

The pulse width is varied in two ways: 1) coarsely, by switching in various sizes of coupling capacitors between dynode and grid, and 2) finely, by varying the grid leak resistors. In the circuit of Fig. 14, the pulse width can in this way be varied in four ranges from 25 mμsec to 12.5 μsec. To make the ranges overlap properly, separate adjustments of the grid bias by potentiometers are provided. Moreover, to compensate for the changes in electrode capacitances from one tube to another, the coupling capacitor is also made variable on the shortest range.

The output of the circuit is taken from the plate of T_3, which serves as an inverter stage. Fig. 15 shows the output pulses for various settings of the width control. The photographs were taken with an oscilloscope having a rise time of 7 mμsec, indicating that the rise time of the pulses themselves was 6 mμsec. The amplitude of the pulses is 17 volts and the maximum repetition rate of the circuit is 10 Mc.

Another version of the secondary-emission circuit is shown in Fig. 16. Here, regenerative action is obtained by coupling together the cathode and the plate of T_2 through the capacitor C_c. The output is taken from the

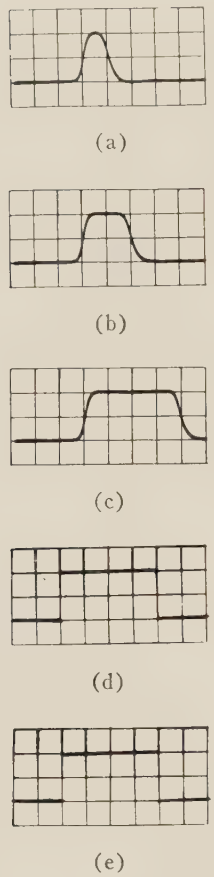


Fig. 15—The output of the secondary emission pulse circuit with the pulse width control set to (a) 25 mμsec, (b) 50 mμsec, (c) 100 mμsec, (d) 1 μsec, (e) 10 mμsec. Horizontal scales: (a)–(c) 25 mμsec/cm, (d) 250 mμsec/cm, (e) 2.5 mμsec/cm.

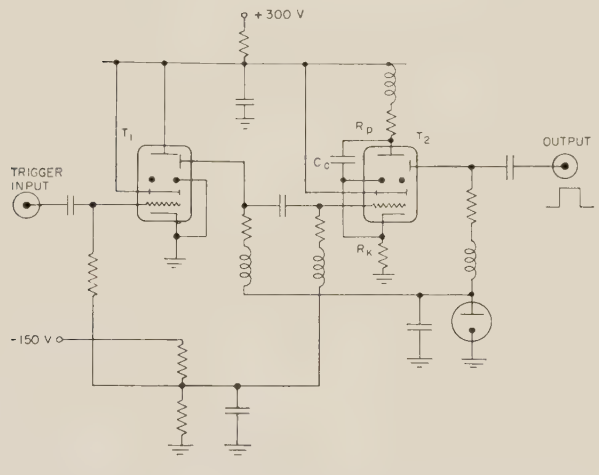


Fig. 16—Another form of the secondary emission pulse circuit.

dynode of the regenerative tube. The minimum pulse width obtainable from this circuit is somewhat smaller than that of the circuit in Fig. 14, since the maximum plate current is larger than the corresponding dynode current and since the total capacitance-to-ground in this case is smaller. On the other hand, however, the pulse width is not so readily varied in this case because of the low cathode input impedance. Hence, this circuit

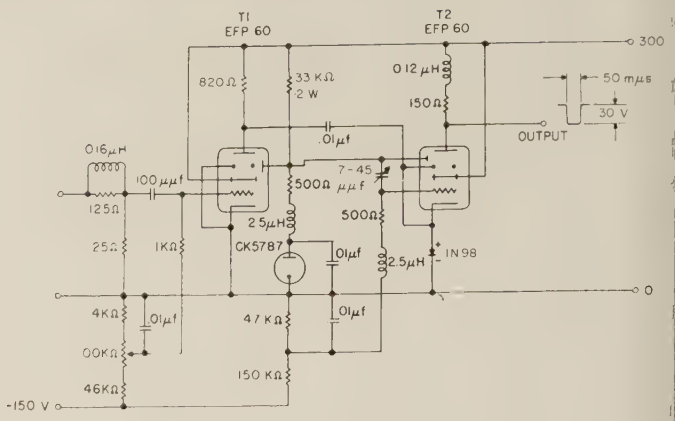


Fig. 17—A fast discriminator circuit.

lends itself best to applications in which the pulse width can be fixed.

The secondary-emission circuit may also be used as a fast pulse-height discriminator. Such a circuit is shown in Fig. 17. With the exception of a few modifications, the circuit is basically the same as that of Fig. 14. The pulse width is here kept constant at about 50 mμsec, and to increase the sensitivity of the circuit, the dynodes of the trigger tube T_1 and the regenerative tube T_2 are connected directly together. The discrimination level is varied by changing the bias of the trigger tube T_1 with a potentiometer. The circuit triggers easily off pulses having a width of 5 mμsec and its maximum sensitivity is 2 volts. The differential sensitivity (the difference between the trigger signal magnitudes at which the circuit operates dependently and just barely reacts) is 0.1 volt. In contrast to many other discriminator circuits, the width of the output pulse is here practically independent of the discriminator-level setting, a feature which highly favors the use of this circuit even when the requirement for speed is not pertinent. For instance, one may readily use it as an FM detector by having it register the positions of the zero crossings.

Conclusions

Two important conclusions may be drawn from the above discussion. First, the fact that the above analysis gives such good agreement with experimental results and so clearly points out the basic properties of such circuits, demonstrates that the method used above is a simple and powerful way of analyzing circuits of this kind. Second, the fact that the term

$$\eta = \frac{I_{ds}}{(E_{cs} - E_{co})C}$$

appears as a factor in all the expressions for pulse width and resolving time indicates that it represents a figure of merit of how well an active device will perform in a switching circuit.

In terms of this ratio, secondary-emission tubes should possess a great potentiality in high-speed pulse circuits since, contrary to ordinary vacuum tubes, it is

ossible in these to increase the saturation current with-
ut too large an increase of circuit capacitance. For in-
ance, with a tube having three dynodes, a pulse circuit
hat is able to generate pulses of between 5 and 10 mμsec
idth and 100 volts magnitude could easily be realized.
should be pointed out, however, that when a large
umber of dynodes are added, the limiting factor will
ot be the ratio η but rather the loop delay introduced
y the time it takes the electrons to go from the cathode
o the last dynode. In the EFP-60 circuit, this delay is of
o consequence since the transit time between the
athode and the dynode is between 2 and 5 mμsec, de-
ending upon the voltage.

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An Electrically Alterable Nondestructive Twistor Memory*

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Summary—**The twistor is a relatively new memory device which may be operated either in a conventional destructive read-out mode, or, by the method explained in this paper, in a nondestructive mode. This paper discusses the basic principles of twistor operation and shows how the twistor may be fabricated into a memory. A nondestructive method of reading a twistor memory by the use of multiple solenoids is described. A typical configuration of a twistor memory which, by the use of this nondestructive reading method, may be operated either in a destructive mode or in a nondestructive mode, is shown.**

Introduction

IN mid-1957 the development of a new memory element was announced by the Bell Telephone Laboratories. Designated the "twistor," the new device showed promise of making possible better and more economical random-access memories for digital computers. As a substitution for the conventional square-loop magnetic cores in coincident-current or word-select memory systems, the twistor would require less driving power and would greatly simplify production. The twistor also offers several other significant advantages over core memories, including increased immunity to environmental extremes.

During the twistor study at the Burroughs Research Center, a method was developed which permits the information stored in a twistor memory to be read out without destruction. In previous random-access magnetic memories, including the familiar ferrite core arrays, sensing of stored information was possible only by resetting all elements to a common state; those elements which were in the opposite state would register outputs, while those already in the common state would register no output. In such systems, if continued storage of the sensed information is required, the information must be temporarily stored and then rewritten into the memory in the write part of the read-write cycle. While this is a simple enough procedure, it presents the possibility of losing information between the read and write operations. Such a loss is not critical in the case of working data storage in an arithmetic digital computer since the program can be designed to recognize the loss and recompute the lost data. However, program and constant data cannot be restored if lost; hence, the destructive read-out memory cannot safely be used in a real-time computer for storage of such information whose loss could abort the mission of, for example, an aircraft or a missile. Programs and constants are thus stored in some

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form of nondestructive memory, the most predominant form of which is the rotating magnetic drum. However, a drum does not permit high-speed random access, and it introduces an undesirable mechanical component in an otherwise all-electronic system.

Other forms of nondestructive storage have also been suggested, but have found only limited use. The wired-core storage, which offers high-speed random access and high reliability, is not easily altered, and is therefore usable only in systems where the program is clearly defined and seldom changed.

The development of a nondestructive twistor memory makes possible for the first time a compact, economical, reliable storage system for miniaturized digital computers, with the facility of easily changing the stored information at any time, through electrical connections alone. Thus a computer can be built with all the speed of a completely random-access memory computer and completely flexible program format.

The following sections summarize the operating principle of the twistor, with comparison to conventional magnetic cores, as well as a discussion of the nondestructive read-out technique.

Basic Principles of Twistor Operation

The principle of operation of the twistor is comparable to that of the conventional square-loop magnetic core. Consider the two-winding toroid of Fig. 1(a). For memory applications, winding 1 may be the bit winding for information and sense, while winding 2 may be used for the read-write word drive. The square-loop material is labeled *M*.

If winding 1 is pulled taut, as indicated in Fig. 1(b), no change will be noted in the magnetic characteristics. Now, if the central helical part of the metal in the magnetic path is long enough, the loop of *M*, which serves as the return path, will be supplanted by the return path formed by the relatively low reluctance of the air gap, as shown in Fig. 1(c). Thus the element will still behave like a memory core.

Many of these "cores" can be strung on a one-word drive winding merely by passing them through the same solenoid, or they can be strung on one straight sense line by connecting them in series. The field strength under the solenoid is such that only that portion of the twistor directly under the solenoid will switch when a drive is applied to the solenoid; distant portions will not.

A bit is written onto the twistor by the coincidence of two magnetic fields, one generated by a current through the center conductor, winding 1 (see Fig. 1), and one generated by a current through solenoid winding 2. The bit so written may be read out by a single reverse current through the solenoid. In the destructive read operation, a voltage is induced by the switching of the square-loop material which is sensed across the center conductor.

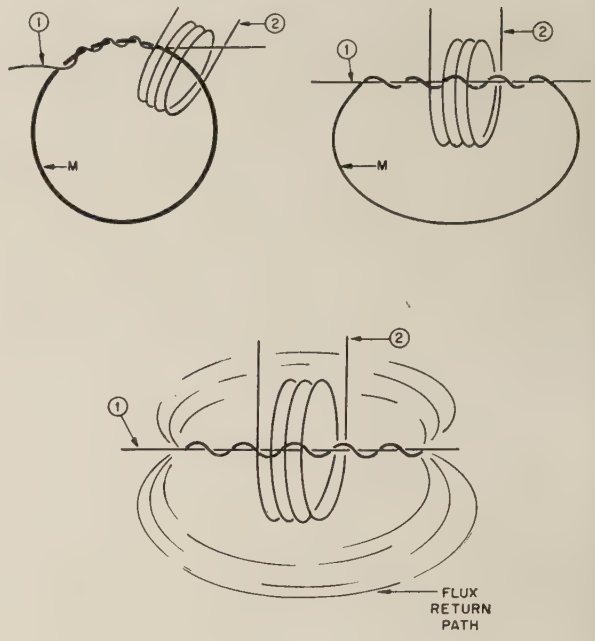

Fig. 1—Twistor-core equivalence.

Twistor Memory Fabrication

The Bell Laboratory version of the twistor in its present state of evolution consists of a flattened wire of square-loop magnetic material wrapped around a central conductor. Burroughs is accustomed to working with molypermalloy tape wrapped around bobbins to form magnetic memory units, and therefore employs tape wrapping to form twistors. Sample memories have been constructed using this tape-wrapped wire (Fig. 2), and have exhibited excellent performance. Special machines have been developed to cut commercially available tape into strips only 0.008 inch wide (tape thickness is 0.000125 inch), and to wind the tape onto the wire.

Since twistor wire may be manufactured in very long lengths, fabrication of the memory array is considerably simplified. For *n* words of *m* bits each, *m* lengths of twistor wire are used. The *m* lengths of twistor wire, after being checked in a continuous tester, an adjunct of the fabrication equipment, are laid parallel between two polyester tapes which are then heat-sealed to form a ribbon. This ribbon is cut so that it is long enough for 64 words. Machine-wound solenoids are slipped over this tape and the tape simply folded back and forth to form a stack with eight words in each layer, eight layers high. This 64-word unit may be combined with as many other 64-word units as required to form *n* words. Fig. 3 shows an experimental twistor memory array fabricated in this manner.

A twistor array of five words of three bits each is shown in simplified representation in Fig. 4. Unlike core memories, in which cores must be individually held in place and wired, the individual bit location in twistor memories requires no special fabrication attention.

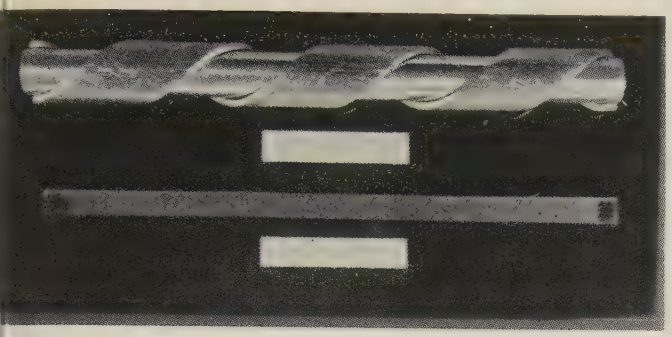

Fig. 2—Twistor element.

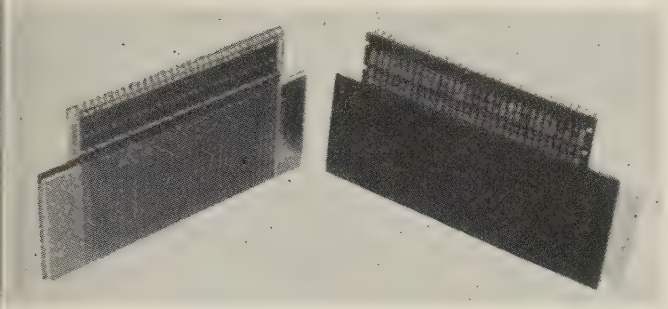

Fig. 3—Twistor memory fabrication.

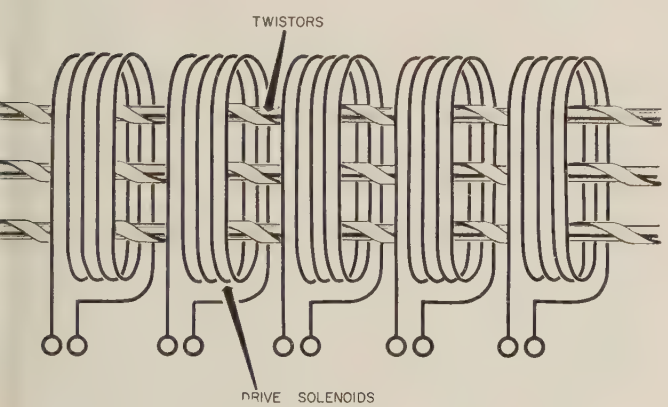

Fig. 4—Five-word, three bit/word twistor array.

Typical Twistor Memory Configuration (Destructive Read-Out)

In a conventional destructive read-out word-select wistor memory, the drive solenoids might be arranged, or selection purposes, in a diode matrix. A four-by-four ersion of the matrix is shown in Fig. 5. The boxes abeled RD supply negative pulses on read, those abeled WD supply positive pulses on write, and those abeled CS (column switches) supply positive on read nd negative on write. The diode matrix has been used uccessfully to drive the small twistor memory men- ioned previously; though it has also been used to drive errite memory cores, the lower currents required by wistors allow more reliable diode operation,

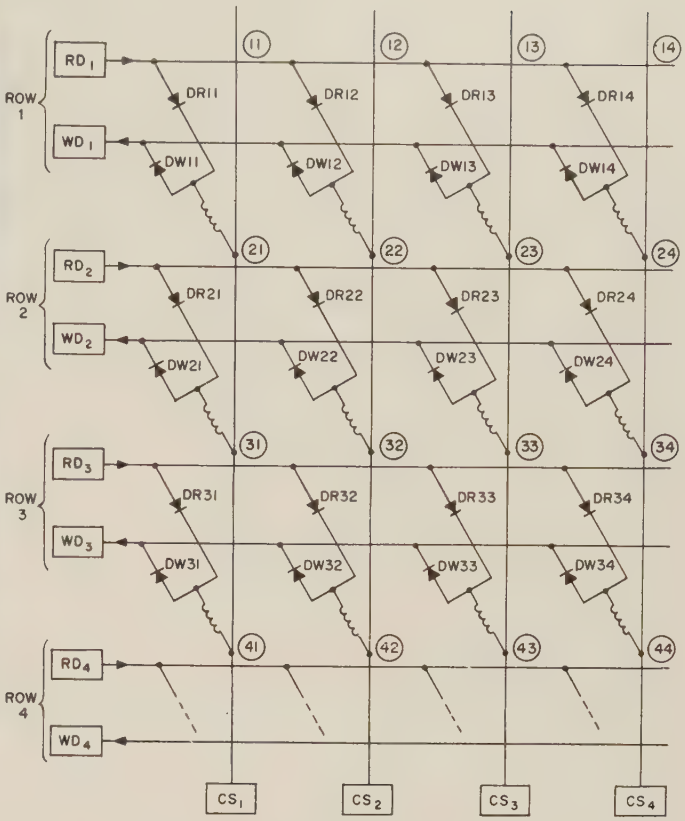

Fig. 5—RAM selector technique.

Nondestructive Read-Out Memory

Experimentation with various methods of twistor/solenoid construction led to a design which permits interrogation of the memory element without destroying the stored information. This feature, not practical with conventional ferrite core arrays, permits the use of a twistor memory in storage systems where loss of information cannot be tolerated.

In a magnetic memory, such as the ferrite core or twistor array, information is read out by pulsing the memory element with an interrogation signal. This signal attempts to switch the device to a common state; if the memory element is already in that state, no output occurs; if in the opposite state, it is switched, the switching action being sensed by an output winding.

Nondestructive interrogation of a twistor element is made possible by several peculiarities of the device. The most significant of these is the fact that the ability of a solenoid winding to switch a section of twistor wire is determined by 1) the size and magnetic characteristics of the twistor itself, 2) the amount of current applied to the solenoid, 3) the length of the solenoid winding, and 4) the magnetic state of the twistor wire on either side of the solenoid. These factors are shown graphically in Fig. 6. It can be seen that for a narrow solenoid, a large difference exists between the current required to switch a twistor when in the ZERO state and the cur-

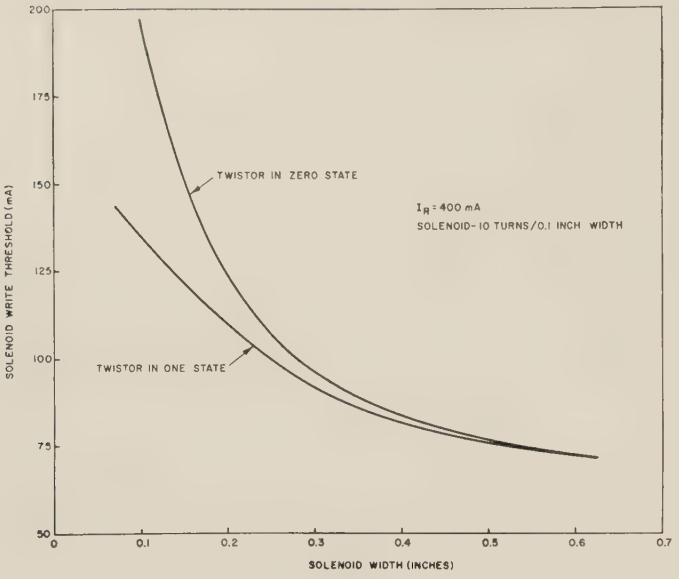

Fig. 6—Twistor performance as a function of solenoid width.

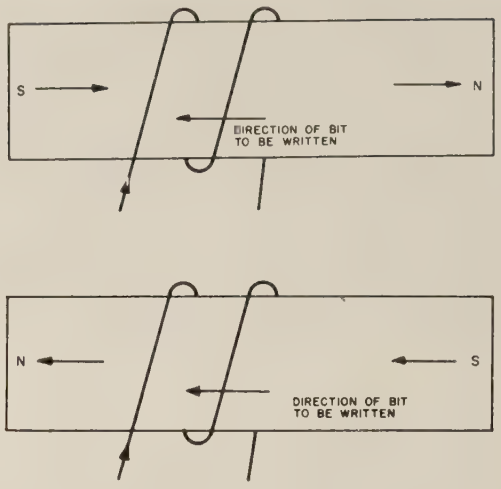

Fig. 7—Bar magnet—twistor analogy. (a) Magnet storing zero; (b) magnet storing one.

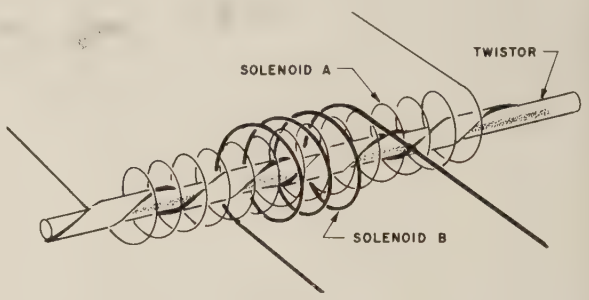

Fig. 8—Nondestructive solenoid windings.

rent required when in the ONE state. As solenoid width is increased, this differential gradually decreases.

The difference in required switching current as a function of the magnetic state can be better appreciated by comparing the twistor to a long bar magnet. Such a magnet is shown in Fig. 7; in this example, flux from left to right represents a ZERO, and flux from right to left represents a ONE. In Fig. 7(a), the flux of the bit to be written is opposed by the flux outside this bit, making write-in difficult. In Fig. 7(b), the outside flux aids the flux of the bit to be written, making write-in easy. Thus, with a write current of proper magnitude and a relatively short solenoid, a bit would not be written if the magnet were storing a ZERO, but would be written if the magnet were storing a ONE.

To make a nondestructive twistor element, a word solenoid is wound, as shown in Fig. 8, with two separate windings. Solenoid *A* is the information entry solenoid and writes by a coincidence of fields in the manner previously described. Its length, and the amount of write current, are such that it sets a section of twistor wire to either of its stable states, representing a stored ONE or a stored ZERO; this initial setting is independent of the previous state of the twistor section. Solenoid *B* is the interrogating solenoid, which tests the state of the wire under it. This solenoid is much smaller than solenoid *A*, and thus samples only a small portion of the total length set by solenoid *A*. The interrogation pulse applied to solenoid *B* causes an output voltage to occur across the twistor if the wire is in the ONE state. If the wire is in the ZERO state, no output voltage occurs. Following the positive-going interrogation pulse, a negative-going reset current of controlled value is then sent into solenoid *B* which resets the small portion of the twistor to the ONE state if a ONE was read out. If a ZERO was read out, the reset pulse has no effect, du to the opposing flux of the surrounding twistor wir Thus the bulk of the twistor section never changes stat after initial information entry. In fact, very recent ex periments have demonstrated that with appropriat twistor design, the reset operation can be eliminate since the small portion of the twistor switched durin interrogation will automatically reset itself to the stat of the surrounding material.

Typical circuit parameters, drivers, and outputs fo the nondestructive read-out system are as follows:

Solenoid *A*, information entry solenoid—40 turns $\frac{1}{2}$ inch wide.
Solenoid *B*, interrogating solenoid—10 turns, 1/3 inch wide.
Interrogating pulse—375 ma.
Reset pulse—95 ma.
Output voltage—20 mv.
Signal-to-noise ratio–4.1.
Switching time—read 0.3 μsec, reset 1 μsec.

The above values are typical of one particular twisto wire in an experimental configuration and do not neces sarily represent optimum operation. Note also that th very short switching times listed above permit a mem ory with a cycle time of less than two microsecond

A complete nondestructive read-out system combining the information insertion solenoid and the interrogating solenoid is shown in Fig. 9.

The information insertion drivers are used only to write in the initial program to be stored. They may then be disconnected and not used, unless it is desired to change the program, which may be done at high speed.

The interrogating drivers are the same type of low-power saturated transistors as those used in a destructive read-out twistor memory.

The advantages of this nondestructive program storage are summarized below:

1) The readout can be either conventional read-write or nondestructive, as desired by the programmer. Stored information is retained indefinitely.
2) Large transients do not affect the stored information since the information insertion solenoids do not operate during readout.
3) The stored information may be changed at high speed whenever desired.
4) The twistor itself should prove highly reliable even in extreme environments.
5) The drive circuits are relatively inexpensive and simple.
6) The mechanical fabrication is simple.

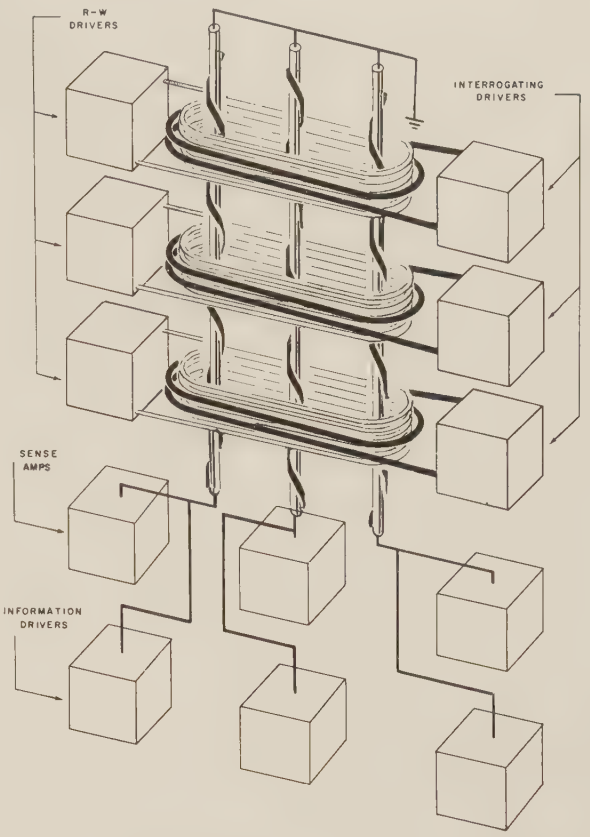

Fig. 9—Twistor nondestructive read-out memory system.

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Current Build-Up in Avalanche Transistors with Resistance Loads*

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Summary—**A transient analysis for the avalanche transistor is carried out through the use of a diffusion model described in terms of charge variables. Basically, the current as a function of time is calculated by taking the gradient of the minority carrier charge stored in the base region. Two methods of approximating the distribution of stored charge are described. Good agreement has been obtained between calculated and experimental results; it is found that the rise time for the resistance-load case is about four times that for a capacitance-load case which produces the same peak current. A practical pulse generator circuit is described in which the resistance load takes the form of a delay-line. The performance of this circuit is compared with that of a capacitance-load relaxation oscillator; while the rise time of the former is longer, the pulse shape is more easily controlled.**

I. Introduction

A MEMBER of the family of high-speed solid-state devices, the avalanche transistor derives its high-speed performance from *avalanche multiplication*, in which charge carriers are multiplied by impact ionization.[1,2] Avalanche transistors have been used to generate high-current fast-rising pulses in sampling oscilloscopes,[3] to provide very short trigger pulses for tunnel diode flip-flops, and to perform as bistable elements with short switching times.[4] It requires little imagination to recognize that these devices provide useful tools for circuit designers in such fields as digital computers, telemetry, and communications.

A previous transient analysis of avalanche transistor circuits has been concerned with the case in which the transistor is used with a capacitance load.[5] Such a circuit produces high-current pulses of short duration, but the pulse shape is not easily controlled. The purpose of the present discussion is to analyze the transient build-up of current in circuits in which the transistor is used with a resistance load. This case includes both bistable circuits and pulse circuits. The discussion is aimed primarily at pulse circuits in which the resistance load takes the form of a delay line, thus providing control o the pulse shape.

Analysis of the current build-up proceeds as follows

1) Approximations are made to obtain a simplifie circuit model.
2) The transistor itself is represented by a diffusio model, *i.e.*, a model in which current flow in th base region is due to the gradient of minority car riers stored there. Basic equations are written i terms of charge variables and the multiplicatio factor M. These equations relate the incrementa charge and voltage at the terminals of the devic to the incremental minority carrier charge store in the base region.
3) Suitable approximations are made regarding th distribution of the stored charge as a function o the current in the terminals. These approxima tions yield equations which may be graphicall integrated to obtain the current as a function o time. Good agreement has been obtained betwee calculated and measured values.

To demonstrate the degradation of rise-time tha must be endured to obtain the increased control o pulse shape through use of the delay line, rise-times ar compared for capacitance- and resistance-load case which would attain the same peak currents. A practica embodiment of the delay-line pulse generator is als described.

II. Circuit and Device Models

The basic circuit of the delay-line pulse generator i shown in Fig. 1. It is assumed that at $t=0$ the line ha been charged to a voltage V_0 by current through R_c At the collector junction of the transistor, the initia voltage V_0 is of sufficient reverse bias to cause ava lanche multiplication, and at $t=0$ the emitter junctio becomes forward biased and injection into the bas begins. A regenerative condition ensues, and the curren builds up rapidly; the collector voltage rises to a valu V_p. Regeneration now ceases, and both voltage and cur rent remain stable until a reflected pulse returns fro the open-circuit end of the line. At this time (if initia conditions were fortuitously chosen), both voltage an current go to zero, and no further reflections occur.

Several assumptions can be made at the outset t simplify the analysis. Usually the peak current flowin into the line is orders of magnitude larger than eithe of the currents through R_b and R_c; it is thus reasonabl to neglect both of these latter currents during the build

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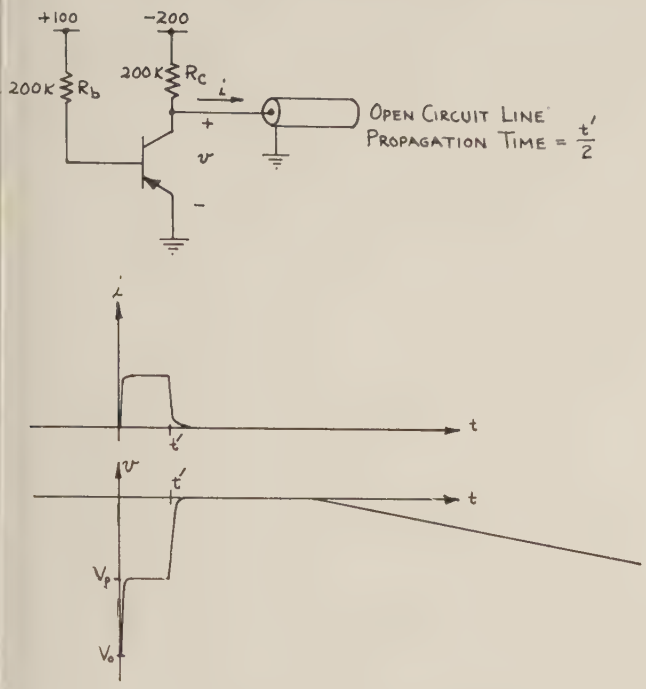

Fig. 1—Pulse circuit and waveforms.

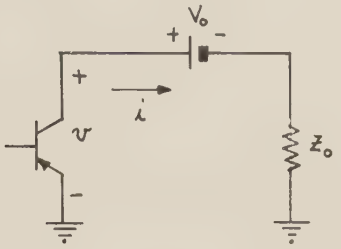

Fig. 2—Simplified circuit model during current build-up.

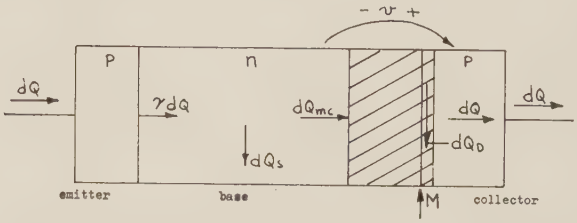

Fig. 3—Diffusion model for the avalanche transistor showing charge variables.

ip period. The build-up of current in the line is suffiiently rapid that the line appears to the transistor as a esistance of value Z_0 (the characteristic impedance of he line). The model of the circuit to be used in the anlysis is shown in Fig. 2, where V_0 is the initial voltage o which the line is charged.

The model of Fig. 3, which is used for the avalanche ransistor, is fundamentally the same as that which is generally used for the analysis of the ordinary diffuion transistor. To the diffusion model is added avaanche multiplication in the depletion region of the collector junction. The following assumptions and approximations are used in the analysis:

1) Space-charge neutrality applies in the base region between emitter and collector depletion layers. Current flow by majority carriers is permitted, but the current flow is governed by the diffusion of minority carriers in the base region.
2) Carrier recombination will be neglected.
3) The emitter junction voltage is negligible, and all of the voltage v appears across the collector depletion layer, whose capacitance is C_c.
4) Avalanche multiplication occurs instantaneously and only at the metallurgical collector junction. The multiplication factor is given by

$$M = \frac{1}{1 - (v/V_B)^n},$$

where V_B is the breakdown voltage, and n is a number (approximately 3) which depends upon the type of material and the type of impurity.
5) During the build-up of current, the nondepleted base width remains fixed at W.
6) The emitter efficiency γ is constant.
7) The transit time for carriers in the depletion region is negligible in comparison to their transit time in the base region.

Since current flow relies fundamentally upon diffusion by minority carriers, it is convenient to describe the behavior of the model in terms of charge variables, as shown in Fig. 3. The appropriate incremental charge variables are defined as follows:

1) dQ is the incremental charge flowing in the external circuit.
2) γdQ is the incremental charge of minority carriers entering the base region.
3) dQ_s is the incremental charge of minority carriers stored in the base region.
4) dQ_{mc} is the incremental charge of holes entering the base side of the depletion layer.
5) dQ_D is the incremental charge of minority carriers which would be required by a change in voltage dv to be deposited in the collector side of the depletion layer. Thus $C_c dv = dQ_D$.

III. Basic Equations

With appropriate charge variables defined, one may write some simple basic equations for the model. A transport factor for the base region may be defined by

$$\beta \triangleq \frac{dQ_{mc}}{\gamma dQ}. \tag{1}$$

Charge continuity in the depletion layer is expressed by

$$M dQ_{mc} = dQ + dQ_D, \tag{2}$$

and charge continuity in the base region is expressed by

$$dQ_s = \gamma dQ - dQ_{mc}. \tag{3}$$

The combination of (2) and (3) yields

$$dQ_s = dQ(\gamma - 1/M) - C_c dv/M, \tag{4}$$

which is the fundamental relation for the device, describing the charge and voltage at the terminals in terms of the charge stored in the base region.

Referring now to the circuit model of Fig. 2, one may write the following in terms of load variables:

$$v = V_0 + iR. \tag{5}$$

Noting that $i = dQ/dt$, and substituting (5) in (4), one obtains

$$dQ_s = (\gamma - 1/M) - RC_0 di/M, \tag{6}$$

where it is to be understood that

$$M = \frac{1}{1 - \left(\frac{v}{V_B}\right)^n} = \frac{1}{1 - \left(\frac{V_0}{V_B} + \frac{iR}{V_B}\right)^n} = \frac{1}{1 - \left(\frac{V_0}{V_B} + \frac{i}{I_B}\right)^n}$$

where $I_B = V_B/R$.

The load current is expressed by (6) as a function of time and the minority carrier charge stored in the base region. To obtain the current as a function of time it is only necessary to find a relationship between current and stored charge. Since current flow in the base is the result of minority carrier diffusion, and since minority carrier diffusion depends upon the gradient of stored minority carrier charge, the necessary relation is obtained by making suitable approximations of the distribution of stored charge and taking the gradient.

IV. Approximation of the Stored Charge Distribution

For practical calculations it is convenient to consider two approximations of the stored charge distribution. The first and simplest is useful when the multiplication factor M is small (near unity) during the entire current build-up. The second is considerably more complicated and is intended for use only when M is large during part of the build-up period.

A. The Small M Approximation

If M is small, the distribution of stored charge will be approximately linear, as shown in Fig. 4. For a linear distribution of charge, the current i_{mc} entering the depletion layer is

$$i_{mc} = Q_s/\tau,$$

where

$\tau = W^2/2D_e$,

D_e = effective diffusion constant for minority carriers,

W = nondepleted base width.

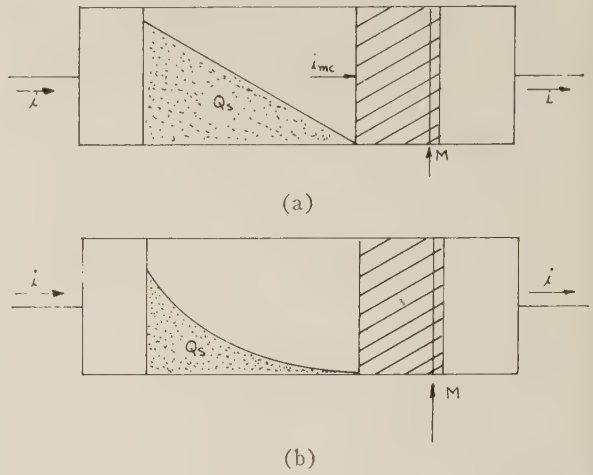

Fig. 4—Stored charge distributions. (a) Linear distribution approximation for small M. (b) For large M, distribution approximated by diffusion equation solution.

The external current is

$$i = Mi_{mc}.$$

Thus the desired relation between i and Q_s is

$$i = MQ_s/\tau. \tag{7}$$

This is, of course, valid only when M is near unity. For example, if $M = 2$, (7) gives a value of i which is about 13 per cent too large.

Eq. (7) may now be differentiated and combined with (6) to obtain a differential equation involving i and t:

$$\tau \frac{di}{I_B}\left\{\left[\frac{1 + RC_c/\tau}{M}\right] - n\left(\frac{i}{I_B}\right)\left(\frac{V_0}{V_B} + \frac{i}{I_B}\right)^{(n-1)}\right\} = \frac{idt}{I_B}\left(\gamma - \frac{1}{M}\right),$$

where $I_B = V_B/R$.

If $RC_c \ll \tau$, RC_c/τ may be neglected in comparison to 1 in (7). To clarify the range of values of R over which this holds true, a typical transistor in which $\tau = 10 \times 10^{-9}$ seconds and $C_c = 5 \times 10^{-12}$ farad is considered. For this case, if R is 200 ohms, $RC_c/\tau = 0.1$. Thus for values of R less than 200 ohms, RC_c/τ may, in this case, be neglected.

Normalized variables I and T, and a function f are defined as follows:

$$I = i/I_B,$$
$$T = t/\tau,$$
$$f = MnI[(V_0/V_B) + I]^{(n-1)}.$$

The differential equation may now be written

$$\frac{dT}{dI} = \frac{(1 - f)}{I(M\gamma - 1)}. \tag{8}$$

It is to be emphasized that M is a function of I, as previously noted.

. Large M Approximation

A solution of the diffusion equation for the base re-ion of the model of Fig. 3 shows that *for a fixed value of ultiplication*, namely M_1, the relation between the ex-rnal current and the stored charge is

$$i = \left(\frac{M_1}{M_1 - 1}\right)\frac{Q_s}{2\tau}(\cosh^{-1} M_1)^2. \tag{9}$$

The approximation is now made that as M varies in he case under consideration, the stored charge in the ase region reaches an equilibrium distribution, given y the diffusion equation solution, more rapidly than I changes. Thus, the relationship between i and Qs approximated by using $M(i) = M_1$ in (9). Differenti-ting (9) and substituting in (6), one obtains

$$\frac{dT}{dI} = \frac{2(\cosh^{-1} M)\left\{(M-1)\left[1 - \dfrac{2Mf}{(\cosh^{-1} M)(M^2-1)^{1/2}} + f\right]\right\}}{I(M\gamma - 1)}. \tag{10}$$

V. Calculation of I as a Function of T

Before calculating I as a function of T, it is instructive o investigate the steady-state value which I will ap-roach for a resistance load R. It can be shown, by a olution of the diffusion equation,[6] that a regenerative uild-up of current will occur as long as $M\beta\gamma > 1$. The teady state will thus be reached when $M\beta\gamma = 1$. If ecombination is neglected, the steady-state value of β s unity, and the steady state will occur when $M\gamma = 1$, .e., when

$$\frac{\gamma}{1 - \left(\dfrac{V_p}{V_B}\right)^n} = 1.$$

The voltage V_p at steady state is given by

$$V_p = V_B(1 - \gamma)^{(1/n)}. \tag{11}$$

If recombination effects are considered, the steady-tate value of the transport factor is β_0 and the condi-ion is $M\beta_0\gamma = 1$. But $\beta_0\gamma = \alpha_0$ where α_0 is the emitter-to-collector current gain of the transistor. When recom-ination is considered,

$$V_p = V_B(1 - \alpha_0)^{(1/n)}. \tag{12}$$

The current in the steady state will be

$$i_{ss} = (V_p - V_0)/R,$$

rom which

$$I_{ss} = (V_p - V_0)/V_B. \tag{13}$$

The calculation of $I(T)$ is most easily accomplished by plotting dT/dI vs I from either (8) or (10), whichever is regarded to be reasonable for the particular case at hand. [The complexity of (10) indicates that its use is to be avoided if possible.] Graphical integration may then be carried out to obtain $T(I)$, and the resulting curve may be replotted to obtain $I(T)$. This has been done for the values shown in Table I, and the result is shown in Fig. 5.

It is worthwhile to estimate how much difference in rise-times exists for a resistance load and a capacitance load which will produce the same peak current. For the resistance load case plotted in Fig. 5 the peak current is $i_{ss} = 162$ ma. Using the equations of Hamilton, *et al.*,[5] for the capacitance case, one finds the peak current given by

$$I_p = CV_B(V_0/V_B)^{(n+1)}/(n+1)\tau.$$

TABLE I

Values Used in the Calculation of $I(T)$

Transistor 2N416

$R = 150$ ohms
$V_0 = -62$ volts
$V_p = -38$ volts
$I_B = -507$ ma.
$\tau = 5.7 \times 10^{-9}$ seconds
$\gamma = 0.962$
$n = 4.7$

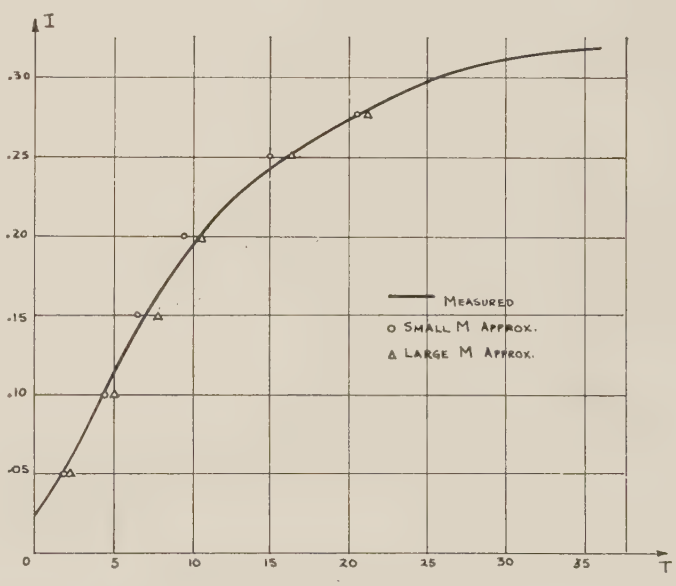

Fig. 5—Calculated and measured current for the transistor of Table I.

For $I_p = 162$ ma, the capacitance required is 222×10^{-12} farad. The estimated maximum and minimum rise-times can be calculated,[6] and are shown in Table II. The rise-time for the resistance case will be about four times that for the capacitance case.

[6] D. J. Hamilton, "A Theory for the Transient Analysis of Ava-anche Transistor Pulse Circuits," Solid State Electronics Lab., Stanford Electronics Labs., Stanford University, Stanford, Calif., Tech. Rept. No. 1701–1; June 15, 1959.

TABLE II

COMPARISON OF RISE-TIMES FOR CAPACITANCE AND RESISTANCE LOADS

Resistance load (150 ohms)	10 per cent to 90 per cent rise-time $= 128 \times 10^{-9}$ seconds
Capacitance load (22 $\mu\mu$f)	
Estimated maximum rise-time 10 per cent to 90 per cent	$= 57 \times 10^{-9}$ seconds
Estimated minimum rise-time 10 per cent to 90 per cent	$= 22 \times 10^{-9}$ seconds

VI. A Practical Pulse Generator

The utility of the delay-line pulse generator circuit of Fig. 1 is limited by the fact that the maximum current is determined by Z_0, a parameter which is not easily adjusted. Further, unless V_0 is chosen so that $V_0 = 2V_p$, reflections which are undesired will occur after the current pulse. The first limitation can be remedied to some extent by paralleling several delay lines of the same length, to decrease the effective Z_0. The second limitation is overcome by inserting resistance in series with the line.

A practical embodiment of an astable delay-line pulse generator is shown in Fig. 6. Here two ends of a single line are connected together to provide the equivalent of two lines, each half the length of the single line, in parallel. Resistance R_1 is inserted to obtain an output voltage proportional to the current, and R_2 is inserted to make the initial voltage transient across the line equal to $V_0/2$. When the reflected transient returns, the net voltage across the line is zero. Both junctions of the transistor are forward biased because of stored charge in the base region, and the collector-to-emitter voltage is approximately zero. Thus, the current through R_2 is approximately zero at that time, and the boundary conditions required by the line for no reflections are met. The value of R_2 is determined from

$$R_1 + R_2 = Z_0'\left(1 - \frac{2V_p}{V_0}\right),$$

where Z_0' is the effective Z_0. R_b and R_c and the supply voltages are chosen to provide the desired repetition rate. The circuit can, of course, be easily arranged for monostable operation.

VII. Conclusion

While the analysis presented here has been cast in terms of a delay-line pulse generator circuit, it is to be emphasized that the same method of attack can be applied, in general, to any avalanche transistor whicl uses a resistance load. Results of the analysis have beer found to be in good agreement with measured data

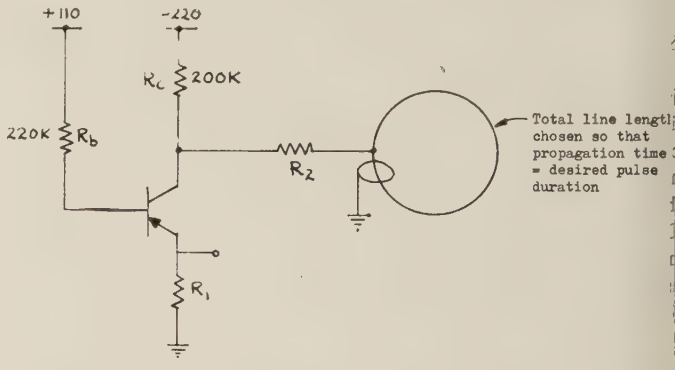

Fig. 6—Practical astable delay-line pulse generator.

The curve of Fig. 5 shows that for the particular case considered, very nearly the same results were obtained from both the large M and small M approximations This is in order, since M was never greater than 2.8 for that particular case. In general, one observes from the functional behavior of M that for a resistance load, M will be small over the bulk of the current range from zero to maximum, and one therefore prefers to use the small M approximation in order to avoid the cumbersome computations required by the large M approximation.

The use of a delay line as a load provides greater control over the pulse duration, amplitude, and shape, and greater freedom from dependence upon transistor parameters, than does use of a capacitor. The price paid for these advantages is an increase in the rise-time. If the pulse generator is to be used only as a trigger, rise-time is more important than pulse shape, and a capacitance load should be used. If, on the other hand, the application is one that demands control of pulse shape, such as a core driver, then a delay line should be used.

High-Speed Transistorized Adder for a Digital Computer*

FORREST SALTER†

Summary—An adder is described that has been developed for the Floating Indexed Point Arithmetic Unit, FLIP, to be used in conjunction with GEORGE, the existing computer built at Argonne National Laboratory. The logic of the high-speed adder and the special circuits required are presented. The adder is parallel and its high speed is made possible by reducing the carry propagation time. Each bit of the adder contributes one transistor to make up a tall AND gate which reduces the carry propagation time to 0.2 μsec. Using this high-speed carry propagation and rather common RCTL transistor circuitry, it is possible to complete an addition in less than 25 μsec.

Introduction

THE ADDER discussed here is a full parallel 68-bit binary adder having three inputs, A, B, and C_{in}, and two outputs, SUM and C_{out}. The adder is a part of FLIP, Floating Indexed Point Arithmetic Unit, which is an all-transistor machine having no core memory or input-output equipment of its own. FLIP will be controlled through GEORGE, a 40-bit vacuum tube computer, and share its 4096 word-core memory.

In some cases a carry must be propagated from the least to the most significant bit. Since the carry propagation normally requires the largest portion of the total add time, the logic is arranged in such a way that carry propagation time is reduced.

Principle of Operation

The principle of operation of this adder can be best understood by reviewing the requirements of a full adder as seen in the truth table, Table I.

The truth conditions are as follows:

1 is the condition of zero volts, appreciable current.
0 is the condition of negative volts, no current.

TABLE I
Truth Table for Full Adder

Line	A	B	C_{in}	C_{out}	SUM
1	0	0	0	0	0
2	0	0	1	0	1
3	1	1	0	1	0
4	1	1	1	1	1
5	0	1	0	0	1
6	0	1	1	1	0
7	1	0	0	0	1
8	1	0	1	1	0

If the A and B inputs are the same (A and B equal "0" or A and B equal "1" as seen in lines 1, 2, 3, and 4), then C_{out} is not dependent on C_{in}. In these four cases there is no need to wait for a carry input from previous stages, since the A and B inputs determine what C_{out} should be. If A and B are 0, then C_{out} should be 0. If A and B are 1, then C_{out} should be 1.

In lines 5, 6, 7, and 8 where A and B are different, we see that C_{out} will be the same as C_{in}. In these cases a true C_{out} cannot be generated in a stage until C_{in} has propagated to that stage. Since the C_{out} will be the same as C_{in}, no inversion is required and the same signal could be passed from C_{in} to C_{out}.

The carry portion of the truth table could be satisfied by a carry switch and switch control box; a block diagram of these two elements is shown in Fig. 1.

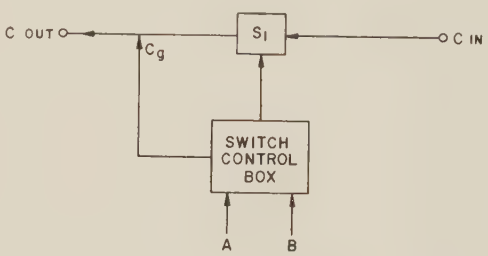

Fig. 1—Block diagram of the basic carry switch.

If A and B are the same, the switch control box should open switch S_i and generate a carry or a noncarry at C_g. If A and B are both 0, then C_g should be pulled to zero. If A and B are both 1, then C_g should be pulled to 1.

If A and B are different, the switch control box should close S_i and not control C_g. This would allow C_{out} to be the same as C_{in}.

In a 68-bit adder there would be 68 carry switches connected in series, each with its own controls. Since all bits of the adder receive their A and B input at the same time, the carry switches will be controlled at the same time. After the switches are set, a signal will travel down the carry line made up of switches S_i until it reaches a stage where switch S_i is open. Here that signal is terminated since a carry or a noncarry has already been generated at this stage.

The Electronic Circuitry

So far, we have treated S_i as a perfect switch, zero resistance when closed and infinite resistance when open. Unfortunately such a switch (that can also be controlled

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† Argonne National Laboratory, Argonne, Ill.

at high speeds) does not exist. In practice a microalloy transistor type 2N393 is used.

Fig. 2 shows some of the transistor switches S_i and their controls connected in series to form the carry line.

The base of each transistor switch is controlled by other transistor circuitry shown here only as a box that will be described later. The transistors in the carry line are operated in the saturated mode, which is slower than nonsaturated operation, but allows V_{CE} to be a minimum. The high speed of the carry line is made possible by controlling all the bases at the same time.

The only current the carry transistors are required to carry is the sum of the base currents of the transistors above it. With 68 transistors in a line, the bottom transistor would be required to carry 68×0.6 ma or 40.8 ma.

Although the 2N393 is capable of handling 40.8 ma, this current would cause rather high collector-to-emitter drops, particularly in the lower transistors. For this reason the carry line is broken into ten sections of seven transistors each. Between each section a pair of emitter followers is placed, which prevents the base currents of one section from passing into the section below it. The emitter followers also shift the signal level positive to help compensate for the negative shift found in the transistor switches below it. Two disadvantages of the emitter follower are a 4-mμsec loss in time and a 5 per cent loss of signal swing. A carry propagated through the entire 68-bit adder might be attenuated from -3.5 volts to -2.5 volts, but with the positive shift of the emitter followers the signal still swings between -2.5 and 0 volts.

A complete schematic diagram of one bit of the 68-bit adder is shown in Fig. 3. When A and B are alike, circuit Section P or Section N will control the "Carry out" line of that stage. In Section P, resistor R_1 drives the "Carry out" to 1 through D_3 if A and B are both 1. This satisfies lines 3 and 4 of the truth table. In Section N, emitter follower No. 12 pulls the "Carry out" line negative when both A and B are negative to generate a noncarry of 0, which satisfies lines 1 and 2 of the truth table. In both cases just mentioned, where A and B are alike, transistor No. 14 is not conducting. The base of transistor No. 14 is controlled by an exclusive-or circuit, made up of transistors No. 1 and No. 2, and an inverter, transistor No. 9. If A and B inputs are different (lines 5, 6, 7, and 8 of the truth table), then transistor No. 14 will be conducting and "Carry out" will be the same as "Carry in."

Transistor No. 9 is a special inverter, which provides fast turn-off for T_9 and allows transistor No. 14 to be turned on fast, yet with limited base current.

Transistor No. 10 is used as an emitter follower to prevent loading on the carry line. Transistor No. 6 is an inverter which both inverts and restores a degenerated "Carry in" signal. Transistors No. 4 and No. 5 form another exclusive-or circuit, whose output is the sum.

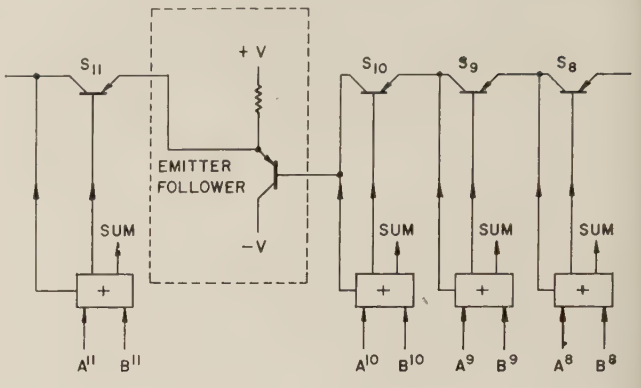


Fig. 2—A portion of a carry line and its controls. All transistors, 2N393.

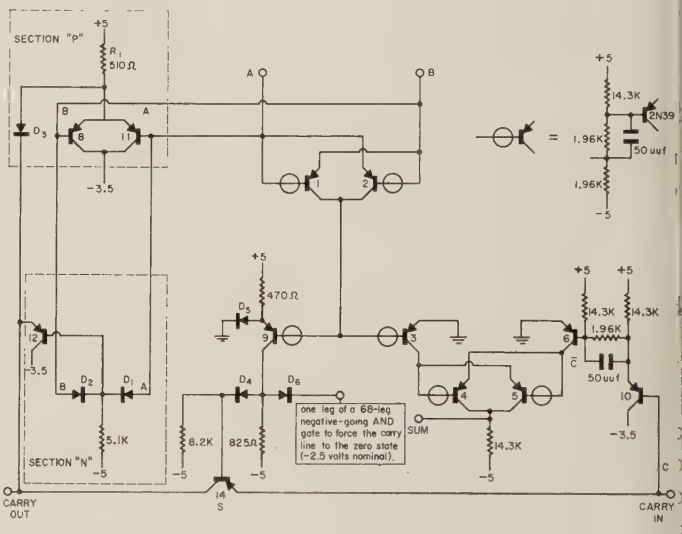


Fig. 3—Schematic diagram of a single full adder stage.

The carry propagation time of the 68-bit adder with the carry propagating through each carry transistor, T_{14}, is about 0.2 μsec. With the addition of some hardware it is possible to bypass groups of carry transistors, providing each bit in that group is to propagate a carry. Selecting a group size of 14 bits, which gives a total of five such groups, the maximum number of carry transistors a carry would propagate would be 29, as compared to 67 without bypassing. This reduction in carry transistors decreases the carry propagation time. This system may be incorporated later, but the results shown in this report do not include the bypass network.

A block diagram of the system used is shown in Fig. 4. Blocks 1 and 2 are the two registers that are always tied to the adder. Block 3 is the complete adder shown in Fig. 3 minus transistor T_{14} and diode D_6. Block number 4 is a 68-leg negative going diode AND gate. The output of this gate controls the carry line if A and B inputs at each bit are different. Block 5 is made up of 68 carry transistors and is controlled by block 3.

The inverters used to form the logic of the adder are standard building blocks used throughout FLIP. These

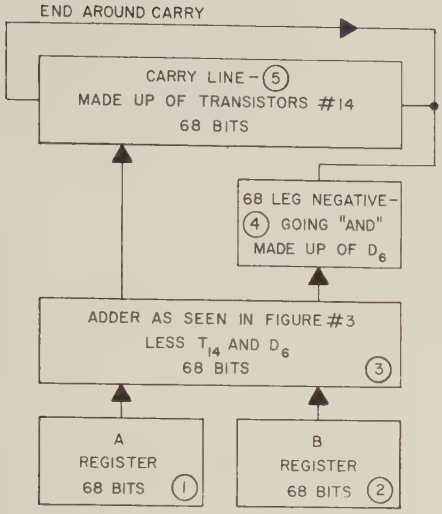


Fig. 4—Block diagram of the complete adder.

verter building blocks have a 20 per cent voltage tol-ance and a 6 per cent resistance tolerance.

Design of a Standard Building Block

The transistor used in the standard building block is e 2N393 germanium microalloy transistor whose ecifications are:

Collector voltage, V_{CB} or V_{CE}: -6 volts (max)
Collector current I_C: -50 ma (max)
Total device dissipation at 45°C: 25 mw (max)
Collector cutoff current, $I_{CBO}(V_{CB}=-5$ volts), typically: 1.5 μa
DC current amplification factor, h_{FE} (after inspection): 45 (min)
Inspection limit: ON condition, $V_{CE}(I_C=18$ ma, $I_B=0.4$ ma): -0.15 volt (max).

The circuitry decided upon was RCTL and is shown Fig. 5. Three equations were derived to solve for lues of R_1, R_2, and R_3 which would give maximum lerance consistent with driving ability.

Since I_{CBO} of T_1 was a maximum of 5 μa at 25°C per ansistor, this current was neglected in the next equa-on, since the computer will be air-conditioned at less an 25°C:

$$I_{B2}^{on} = \frac{V_{B2}^{on} - E_1}{R_1 + R_2} + \frac{V_{B2}^{on} - E_3}{R_3} \cdot$$

The worst condition is when E_1 is low, E_3 high, R_3 w, R_1 and R_2 high. Let a equal the fractional voltage lerance and b equal the fractional resistance toler-ce, then:

$$I_{B2}^{on} = \frac{V_{B2}^{on} - E_1(1-a)}{(R_1 + R_2)(1+b)} + \frac{V_{B2}^{on} - E_3(1+a)}{R_3(1-b)} \cdot \quad (1)$$

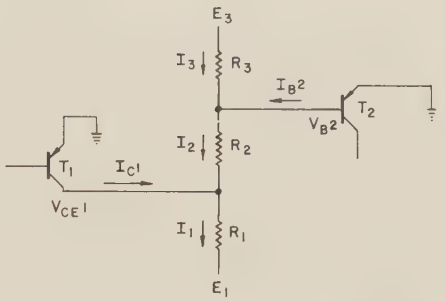


Fig. 5—Schematic diagram of one stage of standard RCTL circuitry. (Arrows indicate conventional current flow.)

Note: $I_{EBO}(V_{EB}=-5$ volts) 10 μa max at 25°C. This current is neglected.

$$V_{B2}^{off} = \frac{E_3(1-a)R_2(1-b) + V_{CE1}^{on}R_3(1+b)}{R_3(1+b) + R_2(1-b)} \cdot \quad (2)$$

$$I_{C1}^{on} = \frac{V_{CE1}^{on} - E_1(1+a)}{R_1(1-b)} + \frac{V_{CE1}^{on} - E_3(1-a)}{(R_3+R_2)(1+b)} \cdot \quad (3)$$

The maximum collector voltage of the 2N393 is 6 volts. For this reason E_1 was selected as -5 volts and E_3 was selected as $+5$ volts. From the transistor characteristics the following operating points were selected:

$V_{B2}^{on} = -0.35$ volt
$V_{CE1}^{on} = -0.13$ volt (max)
$V_{B2}^{off} = +0.3$ volt (min).

Eqs. (1)–(3) were then programmed into the GEORGE computer to find solutions for R_1, R_2 and R_3 as I_{B2}^{on}, I_{C1}^{on} and tolerances a and b were changed.

The solution chosen as the best compromise was as follows:

$I_{B2}=0.4$ ma (minimum base drive)
$I_C=3$ ma (maximum current to control one input network)
$a=13$ per cent (maximum voltage tolerance)
$b=13$ per cent (maximum resistance tolerance)
$R_1=1.956$ K (1.96 K, 1 per cent resistors used)
$R_2=1.968$ K (1.96 K, 1 per cent resistors used)
$R_3=14.27$ K (14.3 K, 1 per cent resistors used).

These calculations were confirmed by actual electrical tests. Although a and b are each 13 per cent, this tolerance could be traded around as long as the total does not exceed 26 per cent. An example might be: resistance tolerance 6 per cent, voltage tolerance 20 per cent. This building block is capable of a fan out of 6, or one collector can drive 6 input networks.

There are two circuits in the adder shown in Fig. 3 that are not standard. One of these is transistor No. 14, the carry switch. This transistor has a special input, to allow its base to remain always more negative than its emitter during conduction. When "Carry in" is driven negative and the base of No. 14 is negative, this tran-

sistor acts as an emitter follower, since it is somewhat bilateral. This allows "Carry out" to be driven negative, providing higher speeds. Transistors 8, 10, 11 and 12 are used as emitter followers to give high speed and current gain.

Experimental Results

The following tests were made on the adder to determine its speed and reliability. The complete 68-bit adder was operated with two double-bank shifting registers, A and B. A program of pulses was generated to cause a three-phase add followed by an error check. If an error is detected a toggle is flipped and the machine is turned off.

The three-phase add consists of the following features.

1) A random number is placed into the lower bank of B register by hand; this number remains here throughout the test. The lower bank of A register is cleared to all zeros. The numbers in A lower and B lower are shifted straight up to A upper and B upper. Since the adder is tied directly to A and B upper, the first add starts at this time. The shift gates are now turned off and A lower is cleared to zero. After enough time has elapsed for carry propagation, the sum of the adder is shifted into A lower. This completes the first phase of the three-phase add.

2) A and B upper are both cleared and the number in B lower is complimented and shifted up left one. This is done simply by gating the other side of B lower one place to the left. At the same time A lower, which is the result of the first add, is shifted straight up to A upper. The gates are turned off and A lower is cleared. The sum of this addition is then shifted into A lower, which completes the second phase.

3) A and B upper are cleared, and A and B lower are shifted straight up. A lower is cleared and the sum is shifted into A lower. Regardless of the number originally placed in B lower, if no mistakes have been made, A lower should contain all 1's. This completes the three-phase add. A fourth period of time was used to test for all 1's, if a mistake had been made in the three-phase add, a toggle is flipped and the control pulses are turned off. A block diagram of the system used to make this test is shown in Fig. 6.

The add time of phase 2 in which the carry propagates 67 bits is shown in Fig. 7. The top waveform in A upper is the bit where the carry is generated, and the bottom waveform is the sum, 67 bits away. The time for this add is 0.23 μsec. The transfer time from A lower to A upper is 0.08 μsec, but is not included in this add time.

The 68-bit parallel adder described here is a reasonable match in speed to the shifting registers and control logic of FLIP. A carry completion system as reported by Gilchrist[1] might reduce the average add time; however,

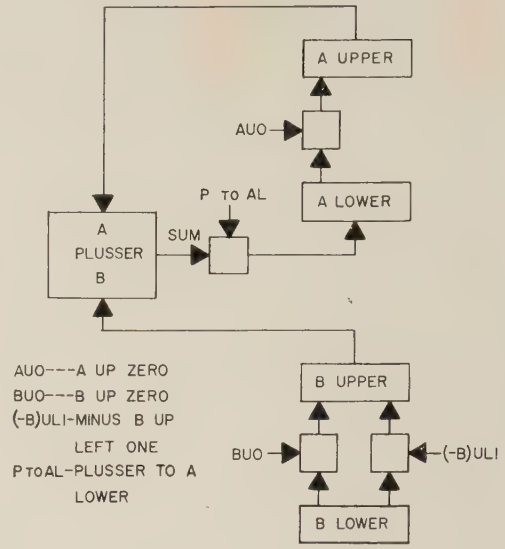


Fig. 6—Block diagram of adder test circuitry (68-bit adder and input registry).

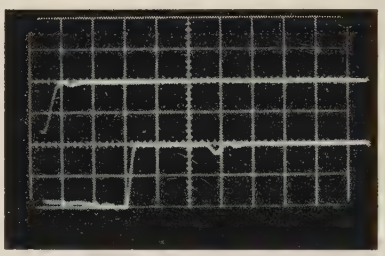


Fig. 7—Waveform of a complete add. (Vertical scale: 2 volts per division. Horizontal scale: 0.1 μsec per division.)

the added hardware necessary would not reduce th maximum addition time, and it is questionable if would be justified in the FLIP system. Gilchrist re ported an average of 0.36 μsec for a 40-bit additio which is longer than the maximum time of 0.23 μsec fo a 68-bit addition reported here.

A more recent transistorized current-routing adde has been reported by Jarvis.[2,3] His adder uses a diod AND gate in the carry line compared to the transisto used in the FLIP adder.

Jarvis reported 0.2 μsec for a 50-bit addition. Th FLIP adder would require 0.17 μsec for this same 50-b addition.

Acknowledgment

The author wishes to express his appreciation t Curtis Rockwood for the encouragement and the wor he did on the standard building block and the test pro cedure for the complete adder system.

[1] B. Gilchrist, J. H. Pomerene, and S. Y. Wong, "Fast carry logic for digital computers," IRE Trans. on Electronic Computers, vol. EC-4, pp. 133–136; December, 1955.

[2] D. B. Jarvis, L. P. Morgan, and J. A. Weaver, "Fast logic usi current-routing and switching techniques," *Digest of Technic Papers*, 1960 Internatl. Solid-State Circuits Conf., Philadelphia, Pa pp. 40–41; February 10–12, 1960.

[3] D. B. Jarvis, L. P. Morgan, and J. A. Weaver, "Transistor cu rent switching and routing techniques," IRE Trans. on Electron Computers, vol. EC-9, pp. 302–308; September, 1960.

Fast High-Accuracy Binary Parallel Addition*

HERBERT C. HENDRICKSON†, MEMBER, IRE

Summary—Future designs of parallel digital computers will be ncerned with increased accuracy in arithmetic operations. When e number of bits per operand is increased, one basic speed limita- n to these operations is the time required to propagate carries in dition or borrows in subtraction. A quantitative method of evaluat- the drastic reduction in time achieved by asynchronous addition hniques is described.

THE basic problem of parallel arithmetic unit design is achievement of high speed and high accuracy at low cost. This paper deals with the design units which achieve higher accuracy by carrying more ts per operand. The model chosen to demonstrate the uantitative evaluation of time savings which can be ade utilizing asynchronous addition or subtraction is e familiar parallel adder shown in Fig. 1. Assume that

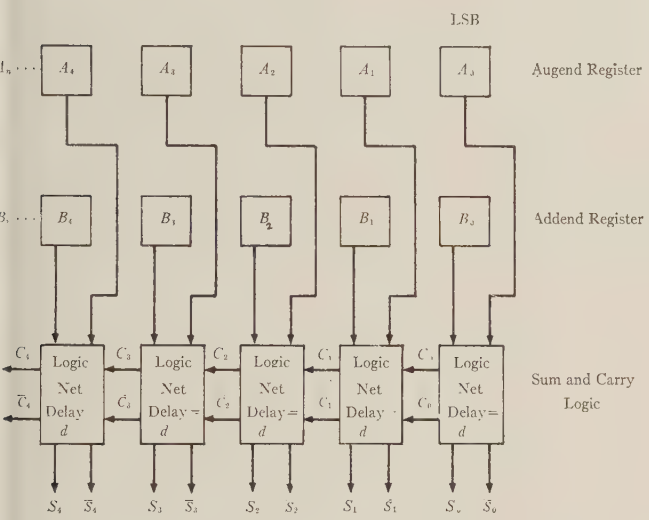


Fig. 1—Model parallel adder.

e parallel adder has n stages. Assume also that the lay in forming C_m or $\overline{C_m}$ out of typical stage m is d icroseconds after the inputs are applied. Obviously, "worst case" design must allow for a sequential delay n all n stages.

Time for longest possible carry $= nd$.

Gilchrist, Pomerene, and Wong[1] suggested a method taking advantage of the cases where carries are set- d in less than time nd. They also scratched the sur- ce of quantitatively determining the amount of time saved. By using a computer, they sampled carry-settling times in additions of pairs of random numbers when $n = 40$. Basically, the time-saving is accomplished as follows:

Let us define A_m as the true output of stage m of the A register, $\overline{A_m}$ as the complement output of that stage, B_m as the true output of corresponding stage m of the B register, and C_m as the "one" carry out of adder stage m.

Both a "one carry" and a "zero carry" line are provided out of each adder stage m. The logic of the "one carry" line is:

$$C_m = [A_m B_m + (A_m + B_m)C_{m-1}](\text{Operate}).$$

The logic for the "zero carry" line is

$$\overline{C_m} = [\overline{A_m}\,\overline{B_m} + (\overline{A_m} + \overline{B_m})\overline{C_{m-1}}](\text{Operate}).$$

From the above equations, it is apparent that the "one carry" line out of any stage m can be set true as soon as the operate signal is true, if both A_m and B_m are true. Also, the "zero carry" line out of any stage m can be set true when operate goes true if both A_m and B_m are false. In all stages where A_m and B_m are opposite, both the C_m line and the $\overline{C_m}$ line will remain false until either the C_{m-1} line or the $\overline{C_{m-1}}$ line becomes true. Thus, carry propagation can start simultaneously out of all adder stages which have $A_m = B_m$, and the time required to set the "one carry" or the "zero carry" line true out of all stages is reduced to Ld, where L is the largest number of stages in succession which have A_m unequal to B_m. Two problems must be resolved to take advantage of the simultaneous, asynchronous carry propagation feature:

1) How can the fact that all sums have been completed correctly be tested?

2) How long should the interval between synchronous clock pulses be to take maximum advantage of shortened add times, and how much will average add time be shortened?

The solution to the first problem is simple when the following logic is implemented:

$$S_m = (A_m B_m + \overline{A_m}\,\overline{B_m})C_{m-1} + (\overline{A_m} B_m + A_m \overline{B_m})\overline{C_{m-1}}$$

$$\overline{S_m} = (\overline{A_m} B_m + A_m \overline{B_m})C_{m-1} + (A_m B_m + \overline{A_m}\,\overline{B_m})\overline{C_{m-1}}.$$

$$\text{Sum completed} = (S_0 + \overline{S_0})(S_1 + \overline{S_1})(S_2 + \overline{S_2})(S_3 + \overline{S_3}) \cdots (S_n + \overline{S_n})$$

Since any given set of outputs C_m, $\overline{C_m}$, S_m, and $\overline{S_m}$ are all false until the operate signal goes true, each term in the sum completed equation starts out false. As appropriate "one carry" and "zero carry" lines become true as inputs to the logic networks, the appropriate S_m or

* Received by the PGEC, March 28, 1960; revised manuscript eived, July 5, 1960.

† Aeronutronic Division of Ford Motor Co., Newport Beach, lif.

[1] B. Gilchrist, J. H. Pomerene, and S. Y. Wong, "Fast carry logic digital computers," IRE TRANS. ON ELECTRONIC COMPUTERS, . EC-4, pp. 133–136; December, 1955.

$\overline{S_m}$ output will go true and will not change again as long as the adder inputs are held. Thus, if a clock pulse occurs before the sum is completed, the result can be ignored for another clock interval and the sum completed signal again tested. When the correct sum is finally achieved, it can be strobed into the answer register by the next clock pulse, the operate signal can be set false, and the inputs to the adder can be changed.

The second problem of how much time can be saved is more difficult. I am very much indebted to L. W. Beck[2] and C. H. Schardin,[2] without whom this work could not have been accomplished. Basic to the description of the concept of an average longest carry is a definition of longest carry. Table I shows the longest carries which result from the addition of all possible three-bit numbers when both "one carries" and "zero carries" are propagated as described above.

TABLE I

LONGEST CARRIES RESULTING FROM ADDITION OF ALL POSSIBLE COMBINATIONS OF 3-BIT NUMBERS

Augends	000	001	010	011	100	101	110	111	Row Total Longest Carries
000	0	1	1	2	1	1	2	3	11
001	1	0	2	1	1	1	3	2	11
010	1	2	0	1	2	3	1	1	11
011	2	1	1	0	3	2	1	1	11
100	1	1	2	3	0	1	1	2	11
101	1	1	3	2	1	0	2	1	11
110	2	3	1	1	1	2	0	1	11
111	3	2	1	1	2	1	1	0	11
Column Total Longest Carries	11	11	11	11	11	11	11	11	88

It can be seen from the table that the longest carry, the largest number of stages in a row having A_m different from B_m, is recorded at the intersection of the augend row and the appropriate addend column. The total number of cases possible when $m=3$ is $2^{2m}=2^6=64$. From the table, the total of all longest carries is 88. The average longest carry will be defined as the total of all longest carries divided by the total possible number of cases. Thus, in the case of $m=3$,

$$\text{average longest carry}_{(m=3)} = \frac{88}{64} = 1.375.$$

The distribution of the longest carries can be determined from Table I for the $n=3$ case:

per cent of additions having zero-length longest carry $=12.5$,

per cent of additions having one-stage longest carry $=50.0$,

per cent of additions having two-stage longest carry $=25.0$,

per cent of additions having three-stage longest carry $=12.5$.

[2] Members of the Technical Staff, Hughes Aircraft Co., Fullerton, Calif.

A further investigation of tables of all possible add tions of n-bit numbers yields the result that each colum contains the same number of total longest carries in th same distribution. Also, tables derived in a simil manner by counting sequences when A_m and B_m a alike, as in subtraction borrow propagation, yield r sults identical to those for addition. Finally, it was di covered that distribution of longest carries for the $n=$ case can be used to find the distribution of carries f the $n=r+1$ case.

Considering the column where the addend is made u of r zeros (where $n=r$), the distribution of longest ca ries in the corresponding column of the table for th $n=r+1$ case can be determined by the following rule

1) The distribution of longest carries in the first ha of the zero augend column of the $n=r+1$ case is th same as the distribution of longest carries in the enti $n=r$ case.

2) The distribution of longest carries in the thi quarter of the $n=r+1$ case column is the same as th distribution of longest carries in the first half of th $n=r$ case, except that the zero-length carry becomes one-stage carry.

3) The distribution of longest carries in the sevent eighth of the $n=r+1$ case is the same as the distrib tion of longest carries in the third quarter of the $n=$ case, except that all carries less than 2 become equal to

4) The distribution of longest carries in the fifteen sixteenth of the $n=r+1$ case is the same as the distrib tion of longest carries in the seventh-eighth of the $n=$ case, except that all carries less than 3 become equal 3.

5) This method can be extended to the thirty-fir thirty-second, the sixty-third sixty-fourth, the on

TABLE II

RESULTS OF PRELIMINARY AVERAGE LONGEST CARRY DETERMINATION FOR THE ADDITION OR SUBTRACTION OF RANDOM n-BIT NUMBERS

Number of Bits $-n$	Total of Longest Carries in Table Zero Addend Column	Total Cases in Column	Average Longest Carry
1	1	2	0.500 0000
2	4	4	1.000 0000
3	11	8	1.375 0000
4	27	16	1.687 5000
5	62	32	1.937 5000
6	138	64	2.156 2500
7	300	128	2.343 7500
8	643	256	2.511 7188
9	1363	512	2.662 1094
10	2866	1024	2.798 8281
11	5988	2048	2.923 8281
12	12,448	4096	3.039 0625
13	25,770	8192	3.145 7520
14	53,168	16,384	3.245 1172
15	109,381	32,768	3.338 0432
16	224,481	65,536	3.425 3082
17	459,742	131,072	3.507 5531
18	939,872	262,144	3.585 3272
19	1,918,418	524,288	3.659 0919
20	3,910,398	1,048,576	3.729 2461
21	7,961,064	2,097,152	3.796 1311
22	16,190,194	4,194,304	3.860 0430
23	32,893,738	8,388,608	3.921 2931

ndred-twenty seventh one hundred twenty eighth, ., until the fraction of the column remaining unnted is

$$\frac{1}{2^{(r+1)/2}} \text{ for odd values of } r \text{ or } \frac{1}{2^{r/2}}$$

even values of r. The distribution of carries in this t uncounted fraction simplifies as follows:

number of $r+1$ stage carries $=1$,
number of r stage carries $=1$,
number of $r-1$ stage carries $=2$,
number of $r-2$ stage carries $=4$,
number of $r-3$ stage carries $=8$,
number of $r-x$ stage carries $=2x$,

until the total remaining number of cases have been counted. The average longest carry calculated from these distributions for values of n ranging from $n=1$ to $n=23$ is given in Table II. An example of the application of these rules to get the distributions for the $n=15$ case from the distributions for the $n=14$ case is shown in Table III.

One additional source of delay must be considered. The value given in Table II does not include the delay necessary to form the carries out of the stages which have A_m equal to B_m. Even though the carry out of such a stage is independent of the carry in, another delay must be allowed for the formation of the "one carry" or "zero carry" input to the longest carry chain. Assume that the magnitude of this setup delay is also equal to d. As a gross approximation, one should then add another

TABLE III

EXAMPLE OF THE USE OF DISTRIBUTIONS OF LONGEST CARRIES IN THE $n=14$ CASE TO OBTAIN DISTRIBUTIONS FOR THE $n=15$ CASE

A. Distribution of Longest Carries when $n=14$

Longest Carry Length	1 / 1st – 2	1 / 3rd – 4	1 / 7th – 8	15 / 16	31 / 32	63 / 64	127 / 128	128 / 128	Number of Cases	Total Carries
0	1								1	0
1	609	377							986	986
2	2526	1328	927						4781	9,562
3	2400	1167	563	773					4903	14,709
4	1394	653	303	139	464				2953	11,812
5	687	315	143	64	28	248			1485	7,425
6	319	144	64	28	12	5	127		699	4,194
7	144	64	28	12	5	2	1	64	320	2,240
8	64	28	12	5	2	1		32	144	1,152
9	28	12	5	2	1			16	64	576
10	12	5	2	1				8	28	280
11	5	2	1					4	12	132
12	2	1						2	5	60
13	1							1	2	26
14								1	1	14
									16,384	53,168

For $n=14$, average longest carry $=\frac{53,168}{16,384}=3.2451171875$.

B. Distribution of Longest Carries when $n=15$

Longest Carry Length	1 / 1st – 2	3 / – 4	7 / – 8	15 / 16	31 / 32	63 / 64	127 / 128	128 / 128	Number of Cases	Total Carries
0	1								1	0
1	986	610							1596	1,596
2	4781	2526	1705						9012	18,024
3	4903	2400	1167	1490					9960	29,880
4	2953	1394	653	303	912				6215	24,860
5	1485	687	315	143	64	492			3186	15,930
6	699	319	144	64	28	12	253		1519	9,114
7	320	144	64	28	12	5	2	128	703	4,921
8	144	64	28	12	5	2	1	64	320	2,560
9	64	28	12	5	2	1		32	144	1,296
10	28	12	5	2	1			16	64	640
11	12	5	2	1				8	28	308
12	5	2	1					4	12	144
13	2	1						2	5	65
14	1							1	2	28
15								1	1	15
									32,768	109,381

For $n=15$, average longest carry $=\frac{109,381}{32,768}=3.33804321$.

delay to all the values shown in Table II. However, if the longest carry happens to include the least significant bit stage, the carry in will be "wired in" or available without any delay. Thus, the longest carries which do not include the least significant bit must be increased by one, and the longest carries which already include the least significant bit must be left unchanged. A quirk of the binary system makes it possible to compensate the average longest carry for this in a simple manner. By adding one to the preliminary average longest carry shown for a value of $n=r$ in Table II, one gets the exact compensated average longest carry for $n=r+1$. Thus, a table of compensated-average longest carries can be prepared as shown in Table IV. Fig. 2 shows a graph of these results plotted on semilogarithmic paper. Notice that points corresponding to values of n greater than 10 lie on a straight line which can be approximated

TABLE IV

n = Number of Augend Bits	Obtained by Counting and Correcting for Initial Carry In Delay	Obtained from Formula Average Long Carry = $\log_2(5n/4)$
2	1.50	1.32
3	2.00	1.91
4	2.38	2.32
5	2.69	2.65
6	2.94	2.91
7	3.16	3.13
8	3.34	3.32
9	3.51	3.49
10	3.66	3.65
11	3.80	3.78
12	3.92	3.91
13	4.04	4.03
14	4.15	4.14
15	4.25	4.24
16	4.34	4.32
17	4.42	4.41
18	4.51	4.49
19	4.58	4.57
20	4.66	4.64
21	4.73	4.71
22	4.80	4.78
23	4.86	4.84
24	4.92	4.92

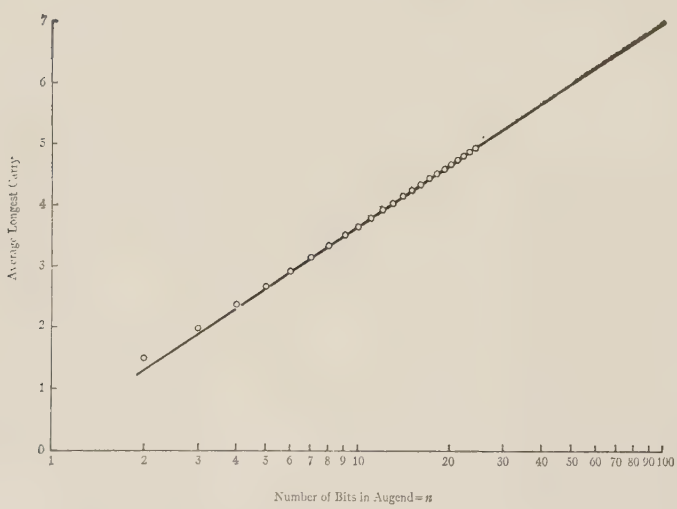


Fig. 2—Compensated average longest carry vs number of bits in augend.

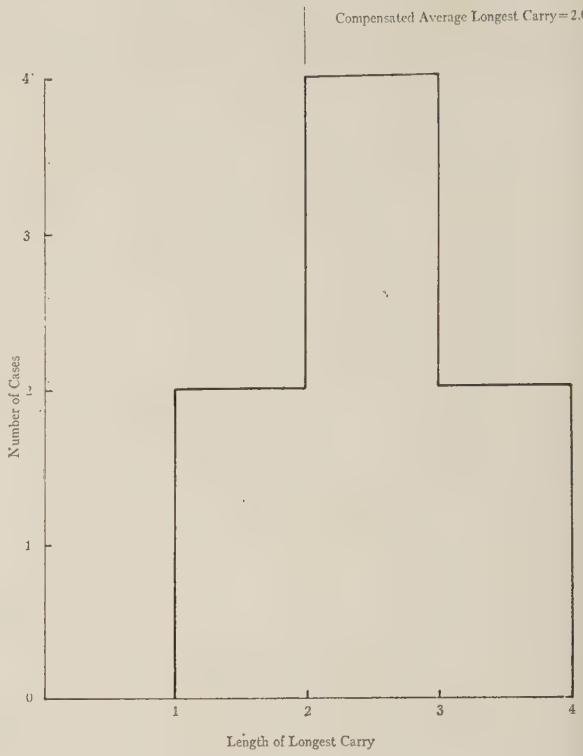


Fig. 3—Distribution of compensated longest carries for $n=$

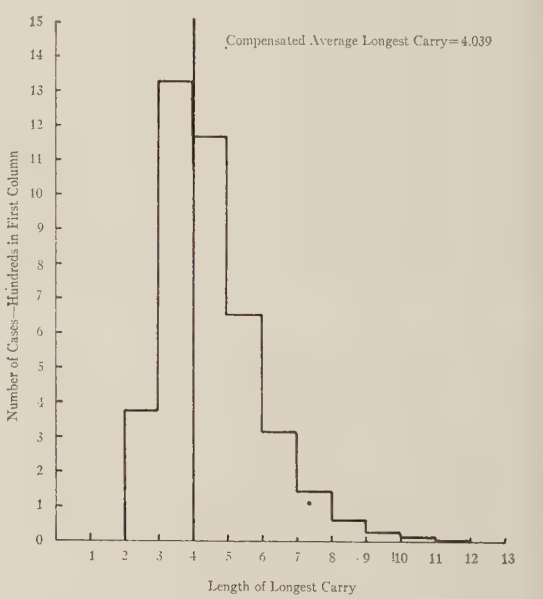


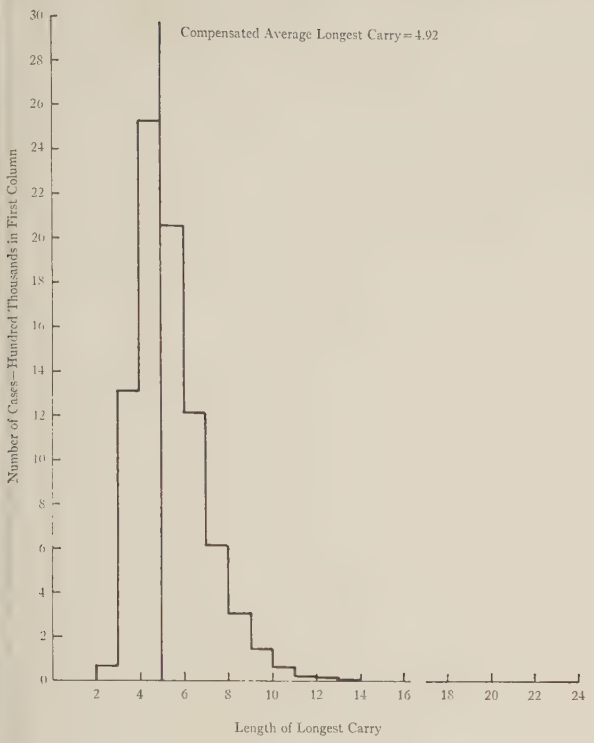
Fig. 4—Approximate distribution of compensated longest carries $n=13$, formed by adding one to all longest carries of $n=12$ case

by the following formula:

$$\text{Compensated average longest carry} = \log_2\left(\frac{5n}{4}\right).$$

Table IV shows a comparison of the values obtained counting and the values obtained by the formula. Burk Goldstine, and von Neumann[3] made an initial investig

[3] A. W. Burks, H. H. Goldstine, and J. von Neumann, "Preli nary Discussion of the Logical Design of an Electronic Computi Instrument," Institute for Advanced Study, Princeton, N. J., vol. pt. I, p. 10; September, 1957.



. 5—Approximate distribution of compensated longest carries for =24, formed by adding one to all longest carries of $n=23$ case.

tion of this problem and estimated the upper bound to be $\log_2 n$, a close though low estimate.

It is interesting to compare the results obtained by Gilchrist, Pomerene, and Wong[1] with those obtained from the formula. By sampling methods, they obtained an average longest carry of 5.6 for $n=40$. By the formula

$$\text{compensated average longest carry}_{(n=40)} = \log_2 \frac{5(40)}{4} = 5.64.$$

Finally, the distributions of longest carries about the average longest must be tested to determine the most effective clock interval to sample the sums. Figs. 3–5 show the distribution curves for the $n=3$, $n=13$, and $n=24$ cases. Notice that for higher values of n, the distribution of longest carries around the average longest becomes quite peaked, indicating that a clock interval equal to slightly more than the product of the average longest carry times d + approximately 3 times d. Extending this technique to high accuracy computers, it should be possible to cut the average add time for a one-hundred bit parallel computer from $100d$ to approximately $10d$ with only a small amount of additional equipment.

Characterizing Experiments for Finite-Memory Binary Automata*

ARTHUR GILL†

Summary—**The characteristics of a discrete automaton with a te memory can be determined by an experiment of a finite length. is paper discusses the properties of such experiments, and pre- ts methods for their optimal construction. Specific results are en for binary-input automata with the memory ranges 0, 1, 2, 3 1 4.**

Introduction

A finite-memory automaton[1] is a sequential machine in which the present output is a function of only a finite number of past inputs. If the input and tput at time t are denoted by x_t and y_t, respec- ely, then an "automaton of memory M" is defined rough the relationship

$$y_t = f(x_t, x_{t-1}, \cdots, x_{t-M}).$$

An automaton of memory M is always equivalent to a strongly connected machine[2] containing $M+1$ states. The characterizing function f, and hence the equivalent machine, can be determined by applying to the given automaton all possible input combinations of $M+1$ symbols. The resulting sequence of symbols constitutes an "experiment" whose "length" equals the number of individual symbols of which it is composed.

The discussion in this paper will be restricted to binary-input automata, where the two input symbols are the digits 0 and 1. The number of combinations to be applied to a binary automaton of memory M for its characterization is given by $C=2^{M+1}$. Denoting the length of the shortest characterizing experiment by

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† Dept. of Electrical Engineering, University of California, keley, Calif.

[1] J. M. Simon, "A note on the memory aspect of sequence trans- ers," IRE Trans. on Circuit Theory, vol. CT-6, pp. 26–29; rch, 1959.

[2] E. F. Moore, "Gedanken-experiments on sequential machines," in "Automata Studies," C. E. Shannon and J. McCarthy, Eds., Princeton University Press, Princeton, N. J., Study 34, pp. 129–153; 1956.

$L_{\min}$, we have

$$M + C \leq L_{\min} \leq (M + 1)C. \qquad (1)$$

The upper bound can always be realized by applying one complete combination after another. The lower bound is realized whenever a sequence can be applied such that, starting with the $(M+1)$th digit, every additional digit completes an $M+1$ digit combination not previously included.

As M becomes large, the ratio between the upper and lower bounds approaches $M+1$. Under these circumstances, the experiment of length $(M+1)C$, although having the simplest composition, becomes highly uneconomical. Special techniques are then desired for the construction of the minimal experiments realizable for the given M, preferably experiments which fulfill the lower bound of (1). Experiments whose length is exactly $M+C$ will be referred to as "compact" experiments.

In a paper by de Bruijn[3] it is shown that a compact experiment is realizable for any M. Moreover, it is shown that the number of compact experiments of the "cyclical" type (which will be discussed later) is, for any M, given by $2^{2^{M}-M-1}$.

The purpose of this paper is to show how compact experiments can be constructed through a graphical approach in simple cases, and through a matrix approach in more complex ones.

Sequential Description of Experiments

Considering an arbitrary combination of zeros and ones, it can be seen that the addition of an $(M+2)$th digit and the deletion of the first digit, results in one of two possible combinations. Designating the original combination by its decimal equivalent n (*i.e.*, the integer which the combination represents when interpreted as a binary number), the new combinations n' and n'' obtained by the described process are given b

$$\left.\begin{aligned} n' &= 2n \doteq C \\ n'' &= (2n \doteq C) + 1 \end{aligned}\right\} \quad n = 0, 1, \cdots, C - 1 \qquad (2$$

where

$$C = 2^{M+1}$$

$$2n \doteq C = \begin{cases} 2n & 2n < C \\ 2n - C & 2n \geq C. \end{cases}$$

Now, regard each $M+1$ digit combination as a discret state (each state labeled with the decimal equivalent o the corresponding combination), and stipulate tha state n directly leads to states n' and n'' if, and only i n, n' and n'' are related as in (2). The result is a s quential system (which depends on M alone, and ha no relationship to the automaton under test), descrik able by a "transition matrix" $T = [t_{ij}]$ as follows:

$$t_{ij} = \begin{cases} 1 & \text{if state } i \text{ leads to state } j \\ 0 & \text{otherwise.} \end{cases} \qquad (3$$

Matrix (4) is a transition matrix for an arbitrary M (fo simplicity, the zeros are omitted). Fig. 1 represents th "transition diagram" for matrix (4).

	0	1	2	3	·	·	·	·	$C-4$	$C-3$	$C-2$	$C-1$
0	1	1			·	·	·	·				
1			1	1	·	·	·	·				
·	·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·	·
$(C/2)-2$					·	·	·	·	1	1		
$(C/2)-1$					·	·	·	·			1	1
$C/2$	1	1			·	·	·	·				
$(C/2)+1$			1	1	·	·	·	·				
·	·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·	·
$C-2$					·	·	·	·	1	1		
$C-1$					·	·	·	·			1	1

(4)

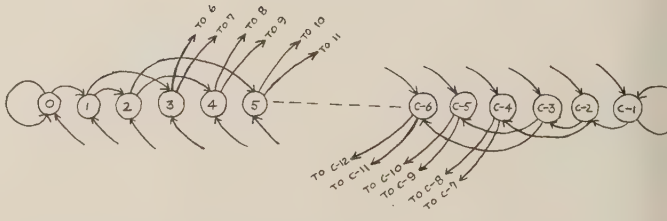

Fig. 1—General transition diagram.

It may now be recognized that every sequence o zeros and ones can be interpreted as a series of trans tions between the states of the sequential system define above. Equivalently, every characterizing experimer can be uniquely associated with some path drawn alor

[3] N. G. de Bruijn, "A combinatorial problem," *Proc. Koninkl. Ned. Akad. Wetenschap.*, vol. 49, pp. 758–764; September, 1946.

e directed branches of the transition diagram for the rresponding M. In particular, any path which tra-rses all the C states can be associated with an experi-ent adequate for characterizing any automaton of emory M. Incidentally, since every combination may ld any other combination (the two may be simply itten consecutively), it is seen that the sequential stem described above is a strongly connected one.

The Minimization Problem

In terms of the description introduced in the preced-g section, the problem of composing the minimal char-terizing experiment can now be formulated as follows. nd the shortest path in the transition diagram such at every state will be traversed at least once. Paths aversing every state exactly once, *i.e.*, "loopless" ths, correspond to compact experiments. An experi-ent can be constructed from the path simply by writ-g the binary equivalent of the first state in the path, d thereafter writing the digits required for the transi-on from one state to the next until the last state is ached.

As an example, consider an automaton of memory 2, here the characterizing experiment is to contain the ght combinations 000, 001, 010, 011, 100, 101, 110 d 111. Matrix (5) is the transition matrix for this ex-mple. Fig. 2 is the corresponding transition diagram.

$$\begin{array}{c|cccccccc} & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 0 & 1 & 1 & & & & & & \\ 1 & & & 1 & 1 & & & & \\ 2 & & & & & 1 & 1 & & \\ 3 & & & & & & & 1 & 1 \\ 4 & 1 & 1 & & & & & & \\ 5 & & & 1 & 1 & & & & \\ 6 & & & & & 1 & 1 & & \\ 7 & & & & & & & 1 & 1 \end{array} . \qquad (5)$$

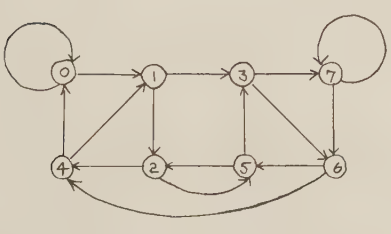

Fig. 2—Transition diagram for $M=2$.

The diagram readily reveals the path 0-1-3-7-6-5-2-4 be a minimal path of the desired properties. The sociated experiment is then 0001110100. Since the th is loopless, the resulting experiment is compact, as n also be verified from (1).

General Solution

The construction of the transition diagram and the acing of the minimal path become more cumbersome as M becomes larger. Under these circumstances, the task of finding the minimal experiment is facilitated by regarding the matrix T, as defined by (3), as an ordinary transition matrix of an unweighted directed net,[4] and then constructing the matrix T^k to yield all paths of length k.

For the purpose at hand, it is convenient to replace every "1" which appears in the ijth position of the matrix by the subscripted symbol t_{ij}. The elements $t_{ir_1}, t_{r_1r_2} \cdots t_{r_{k-1}j}$ appearing in T^k will then place in evidence the vertices $i, r_1, r_2, \cdots, r_{k-1}, j$ traversed by the corresponding path. The construction of the matrices is greatly simplified if the elements in which any r_h equals any other subscript (thus representing a "loopy" path) are eliminated as soon as they appear in the constructed matrix. Consequently, the number of terms in each matrix is considerably reduced, and the main diagonal in T^k contains closed paths only, in which no branch is included more than once. In particular, the main diagonal of T^c would contain all the paths corresponding to the desired compact experiments.

Table I lists compact experiments determined for $M=0, 1, 2, 3, 4$.

TABLE I

M	Compact Experiments
0	01
1	00110
2	0001110100
3	0000111101100101000
4	00000110011111000100101011011010000

Besides being compact, all the tabulated experiments are "cyclical," in the sense that if the first C digits are written around a circle, then any sequence of $M+C$ digits, regardless of the starting point, constitutes a compact experiment. Since any two sequences with different starting points are necessarily distinct, the existence of a compact and cyclical experiment implies the existence of at least C such experiments. It can also be seen that the complement of a compact experiment (where all the zeros are replaced by ones and vice versa) is also a compact experiment.

Conclusions

The preceding sections showed how experiments intended for characterizing finite-memory automata can be viewed as sequential systems in their own right. This view, together with de Bruijn's results and the theory of transition matrices, was found helpful in devising methods for constructing the most economical experiments fulfilling the required characterization task. Specific results were presented which constitute the shortest experiments for automata of memory $M=0, 1, 2, 3, 4$. Experiments for machines with larger memories can be constructed in an analogous manner.

[4] F. E. Hohn, S. Seshu, and D. D. Aufenkamp, "The theory of nets," IRE Trans. on Electronic Computers, vol. EC-6, pp. 154–161; September, 1957.

Statistical Recognition Functions and the Design of Pattern Recognizers*

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Summary—According to the model discussed in this paper, a pattern recognizer is said to consist of two parts: a receptor, which generates a set of measurements of the physical sample to be recognized, and a categorizer, which assigns each set of measurements to one of a finite number of categories. The rule of operation of the categorizer is called the "recognition function." The optimization of the recognition function is discussed, and the form of the optimal function is derived. In practice, a prohibitively large sample is required to provide a basis for estimating the optimal recognition function. If, however, certain assumptions about the probability distributions of the measurements are warranted, recognition functions that are asymptotically optimal may be obtained readily.

A small numerical example, involving the recognition of the hand-printed characters *A*, *B*, and *C* is solved by means of the techniques described. The recognition accuracy is found to be 95 per cent.

Automatic Pattern Recognition

WE SHALL BE dealing with a particular model of a pattern-recognition system. According to this model, a pattern recognizer will be said to consist of two principal parts, a receptor and a categorizer.

Receptor

The receptor has as its input a physical sample to be recognized and as its output a set, $X_1, X_2, \cdots, X_p$, of quantities which characterize the physical sample. These quantities will be called "measurements" of the sample, and the set of measurements will be designated by the letter X.

Categorizer

The output, X, of the receptor constitutes the input to the categorizer. The categorizer is a device which assigns each of its admissible inputs to one of a finite number, m, of categories. We may say that the output of the categorizer is an integer $i=1, 2 \cdots, m$, under the convention that output i is to mean that the categorizer has assigned its input to the ith category among the set of m categories. Thus, we may say that the categorizer computes a function $i=R(X)$.

The function $R(X)$ will be called the *recognition function* of the pattern recognizer. We shall be primarily concerned with the calculation of this function.

Each physical sample will be considered as "actually belonging to" one of the m categories. Whenever a pattern recognizer assigns to category j a physical sam actually belonging to a category other than j, we s that the pattern recognizer has made an *error*.

The Optimal Recognition Function

In a given pattern-recognition situation, we say th a pattern recognizer P_1 *is better than* a pattern recogni P_2 if the probability that P_1 makes an error is less th the probability that P_2 makes an error.

If P_1 is a pattern recognizer having receptor ρ a recognition function R_1, and if P_2 is a pattern recogni having the same receptor ρ but a different recogniti function R_2, and if P_1 is better than P_2, then we s that R_1 *is better than* R_2 *with respect to* ρ.

If a recognition function R is better than, or at le as good as, any other recognition function with resp to a given receptor ρ, we say that R is *optimal with spect to* ρ.

In the discussion that follows, the qualifying phra "with respect to a given receptor ρ," will often omitted for the sake of brevity, and we shall spe simply of a recognition function as being optimal, qualification being understood.

We shall not be concerned in this paper with problem of designing good receptors, that is, of picki good sets of measurements. The receptor will be sumed to be given, and our attention will be focused the recognition function.

We now derive the form of the optimal recogniti function. The result we shall obtain is by no mea novel. We present it here, in somewhat abbreviat form, for the sake of completeness, and also because will help in fixing ideas for the subsequent discussio

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[1] In this and subsequent sections we are following material gi by T. W. Anderson in his "Introduction to Multivariate Statist Analysis," John Wiley and Sons, Inc., New York, N. Y., 1958. facilitate cross-reference we have tried to keep our notation comp ible with his.

The treatment closest to ours in motivation is given by C. Chow, "An optimum character recognition system using decis functions," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-6, 247–254; December, 1957.

Further references are:

A. Wald, "Statistical Decision Functions," John Wiley and So Inc., New York, N. Y.; 1950.

W. W. Peterson and T. G. Birdsall, "The Theory of Signal tectability," Electronic Defense Group, Engrg. Res. Inst., Univers of Michigan, Ann Arbor, Tech. Rept. No. 13; 1953.

D. Middleton and D. Van Meter, "On optimum multiple de tion of signals in noise," IRE TRANS. ON INFORMATION THEORY, IT-1, pp. 1–9; September, 1955.

For a more elementary discussion of some of the relevant conce see:

T. Marill, "Detection Theory and Psychophysics," Res. Lab Electronics, M.I.T., Cambridge, Tech. Rept. No. 319; 1956.

t will be recalled that the receptor generates p asurements, $X_1, X_2, \cdots, X_p$, of each physical mpie. We will write these as a column[2] vector

$$X = \begin{bmatrix} X_1 \\ X_2 \\ \cdot \\ \cdot \\ \cdot \\ X_p \end{bmatrix}.$$

s quantity is the input to the categorizer; it is the ument of the recognition function $R(X)$.

The vector X comes from one of m categories, or opulations," $\pi_1, \cdots \pi_m$. We assume that their *a priori* probabilities are equal, *i.e.*, we assume that it is t as likely that X comes from one population as from other.[3]

The probability distribution of X depends upon the pulation from which X is drawn. We will let $p_i(x)$ the (multivariate) probability distribution (if X is crete) or the probability density function (if X is tinuous) of the variable X when X is from π_i. We thus dealing with m functions $p_i(x)$, $i=1, \cdots, m$. We seek a function, or rule, R, which assigns each X exactly one of the populations π_i.

The conditional probability that a given vector X_0 ually came from population π_j is given by

$$\frac{p_j(X_0)}{\sum_{k=0}^{m} p_k(X_0)}.$$

erefore, the probability that X_0 did not come from s

$$1 - \frac{p_j(X_0)}{\sum_{k=1}^{m} p_k(X_0)}. \qquad (1)$$

a given rule R assigns the vector X_0 to population the probability that this assignment will be in error given by (1).

Now, we build up our desired rule R as follows. Given articular X_0, we calculate (1) m times, once for each ue of j; we have thus calculated the probability of or if R assigns X_0 to π_1, if R assigns X_0 to $\pi_2, \cdots$, R assigns X_0 to π_m; we then pick for incorporation o our desired optimal rule R^* the assignment for ch the probability of error is least.[4] We repeat the cess for each possible value of X. The resultant rule has a minimum probability of error. To put it more cinctly: given a value for X, (1) determines m quantities, one for each $j=1, \cdots, m$. The desired rule R^* assigns the given X to that j for which (1) is least.

We now notice that the value of j for which (1) is least is also the value of j for which $p_j(X_0)$ is maximal. Hence, the desired optimal rule will pick that value of j for which $p_j(X_0)$ is maximal.

In summary, the optimal recognition function, or rule, R^* assigns X to π_i if and only if[5] $p_i(X) > p_j(X)$, $j=1, \cdots, m; j \neq i$.

Practical Considerations. Random-Search and Other Techniques for Approximating the Optimal Recognition Function

When we wish to apply to above theory, we unfortunately stumble into the following difficulty. In general we do not know the distributions $p_i(x)$. Therefore, we cannot calculate the optimal recognition function.

Let us consider what is involved in *estimating* the $p_i(x)$ in the simplest case, namely, the case in which X is discrete and has finite range. Let us say that each of the p components of the vector X can assume one of r values. In this case, each $p_i(x)$ is specified by $r^p - 1$ quantities and the entire set of p_i's by $m(r^p - 1)$ quantities. We can easily envisage a pattern recognition task in which $m = r = p = 10$; in this case the set of p_i's is specified by some 100 billion quantities. This approach leads to impossibly difficult estimation problems.

It is this fact, we believe, that has led some authors[6] to propose random-search techniques for approximating the optimal recognition function. In this technique we search through the ensemble of possible recognition functions; as the search proceeds each recognition function is subjected to tests, the better ones being retained, the worse ones rejected. The search may be entirely random, or it may be organized by imposing various degrees of constraint. As yet very little is known about the efficiency of such techniques.

The technique discussed in the remainder of this paper represents an alternative attempt to come to grips with the problem of the unknown probability distributions. It is the technique, familiar enough to workers in statistics, of making *assumptions* about the nature of these distributions.

Consider the familiar elementary problem of testing the hypothesis H_0 that a given set of measurements was drawn from a population having zero mean. We may employ the following technique. We assume that the underlying distribution is normal, and we employ, say, Student's t-test. If our assumption is correct, we are guaranteed a very powerful test; *i.e.*, given a certain acceptably low probability of rejecting H_0 when it is

[2] The corresponding row vector is the transpose $X' = [X_1 \cdots, X_p]$. ughout the discussion, the apostrophe to the right of a matrix able will indicate the transpose.

[3] This assumption is made here for simplicity. The introduction nequal *a priori* probabilities does not present any severe theoretic difficulty, provided these probabilities are assumed to be known. One may wish to assign different costs to the different kinds of r. Doing so does not present any severe theoretical difficulty. It , however, complicate the model appreciably.

[5] Strictly speaking, if $p_i(X) = p_k(X)$ and $p_i(X) > p_j(X), j=1, \cdots, m, j \neq i \neq k$, then R^* can assign X to either π_i or π_k.

[6] See, for example, O. G. Selfridge, "Pandemonium: A Paradigm for Learning," presented at Mechanization of Thought Processes Symposium, National Physical Lab., Teddington, Eng.; 1959.

F. Rosenblatt, "Perceptron simulation experiments," Proc. IRE, vol. 48, pp. 301–310; March, 1960.

true, the test guarantees a high probability of rejecting H_0 when it is false. If our assumption is false, the guarantee is void.

In attempting to find acceptable recognition functions we shall also use the method of making assumptions about the underlying distributions. The risk involved here, however, is very much *smaller* than in the case of testing a hypothesis by means of a statistical test. When we use a statistical test, we are committed to the outcome of the test; we have no independent way of knowing whether the result of the test is in error. When we find a recognition function, however, we do have such an independent test. We can readily determine whether this function, in conjunction with a given receptor, is acceptable, by testing whether it recognizes patterns accurately.

The technique to be discussed is "algorithmic." This means that it is always possible to say in advance how much calculation is required to find a recognition function. If the assumptions of the model are met, the resulting recognition function is asymptotically optimal; that is, the function approaches the optimal recognition function as the sample size increases. If the assumptions are not met, the recognition function may still be acceptable; or it may not, in which case a prespecified amount of computation will have been wasted.

Solution With Normal Variables and Equal Covariance Matrices[7]

We shall be discussing the solution of the model under two assumptions: 1) that the measurements are normally distributed, and 2) that the covariance matrices of the $p_i(x)$ are equal for all i. In the present section we deal with the more restrictive case in which both assumptions are made. In a later section we return to discuss the model for the case in which only the first assumption is made. (The assumption of statistically independent measurements is *not* made at any point.)

We here assume that the $p_i(x)$, $i=1, \cdots, m$, represent (multivariate) normal densities which differ only in their means.

Specifically, we assume that the probability density p_i of X when X is from population π_i is[8]

$$p_i(x) = \frac{1}{(2\pi)^{p/2} \left| V \right|^{1/2}} \exp\left[-1/2(x-\mu_i)'V^{-1}(x-\mu_i)\right].$$

The ratio of two densities p_i and p_j is given by

$$\frac{p_i(x)}{p_j(x)} = \exp\{-1/2[(x-\mu_i)'V^{-1}(x-\mu_i) - (x-\mu_j)'V^{-1}(x-\mu_j)]\}.$$

Taking logarithms and rearranging terms we have

$$u_{ij} = \log \frac{p_i(X)}{p_j(X)} = X'V^{-1}(\mu_i - \mu_j) - 1/2(\mu_i + \mu_j)'V^{-1}(\mu_i - \mu_j). \quad (2$$

It will be recalled from the previous section that a optimal rule R assigns X to π_j if $p_j(X)$ is the large among the $p_i(X)$. In terms of the function u_{ij}, this ru is:

> Form the $m(m-1)$ quantities u_{ij}, $(i=1, \cdots, m; j=i, \cdots, m; i \neq j)$ and pick the largest of these quantities. If the largest is u_{kj}, assign X to π_k. (

Proof: By this rule, one is to pick the largest of t $m(m-1)$ quantities

$$u_{ij} = \log \frac{p_i(X)}{p_j(X)} = \log p_i(X) - \log p_j(X) \quad (i = 1, \cdots, m; j = 1, \cdots, m; 1 \neq$$

The largest of these u_{ij} is formed by taking the large among the m quantities $\log p_i(X)$ and subtracting t smallest. Hence, the first subscript of the largest will be the same as the subscript of the largest $p_i(X)$, which in turn is the same as the subscript of t largest $p_i(X)$. Hence, our present rule, (3), is equivale to the rule:

> Pick the largest of the m quantities $p_i(X)$. If this is $p_k(X)$, assign X to π_k. (

This latter rule, (4), is the one which was seen in t previous section to be optimal.

In summary, we consider a vector quantity X whi comes with equal probability from any of m popul tions $\pi_1, \cdots, \pi_m$. The populations π_i are assumed be normally distributed with mean vectors $\mu_1, \cdots$ μ_m, and with equal covariance matrices, V.

Under these assumptions, the optimal procedure is form the $m(m-1)$ functions

$$u_{ij} = X'V^{-1}(\mu_i - \mu_j) - 1/2(\mu_i + \mu_j)'V^{-1}(\mu_i - \mu_j)$$

to pick the largest, say u_{kj}, and to assign X to π_k.

An aspect of the present technique which is partic larly appealing is that the functions u_{ij} are *line* functions of X. The recognition function is thus e tremely simple to instrument.

Even with the assumptions of normality and equali of the covariance matrices, there are still estimati problems involved in the present model, although n very severe ones. Where, as before, p is the number measures and n the number of categories, the number independent quantities to be estimated is equal $mp+\frac{1}{2}(p^2+p)$. For $m=p=10$, this is equal to 155.

[7] In this section we are, once again, relying to a considerable extent on material given by Anderson, *op. cit.*

[8] The expression $|V|$ represents the determinant of the covariance matrix V, *i.e.*, of the matrix whose elements, cov_{ij}, represent the covariance between the ith and jth component of the vector X. The diagonal element cov_{ii} represent the variance of the ith component.

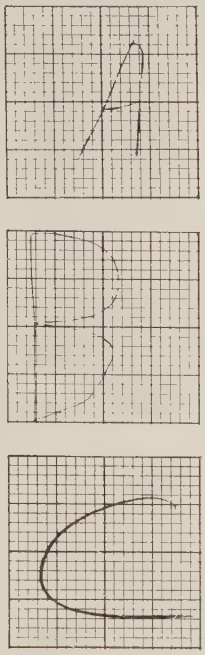

Fig. 1—Examples of letters obtained from subjects.

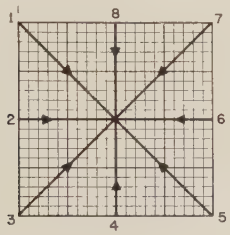

Fig. 2—Grid used in forming measurements of letters.

A Numerical Example of the Above Technique

Experimental Situation

As an example of the technique sketched in the previous section, a very simple pattern-recognition task was carried out. The problem consisted in recognizing the hand-printed characters A, B, and C. Five samples of each letter were obtained from each of ten subjects; thus, 150 letters in all were processed.

The subjects were instructed to print the letters within a two-inch square. Examples of letters obtained are given in Fig. 1.

Measurements were made on the letters as follows. A grid of four intersecting lines (see Fig. 2) was placed on the square in which the letter was written. Measurement X_i consisted in determining how far one need travel along the directed line segment i before intersecting a portion of the letter for the first time. In this fashion eight measurements, $X_1, \cdots, X_8$, were made of each letter (see Fig. 3). Since the letters were written on graph paper with 1/10 inch ruling, the measures could be read off the paper simply by counting small squares. Measurements 1, 3, 5, and 7 (along diagonals) were in units $\sqrt{2}$ larger than the units of measurements 2, 4, 6, and 8. No correction for this discrepancy was applied.

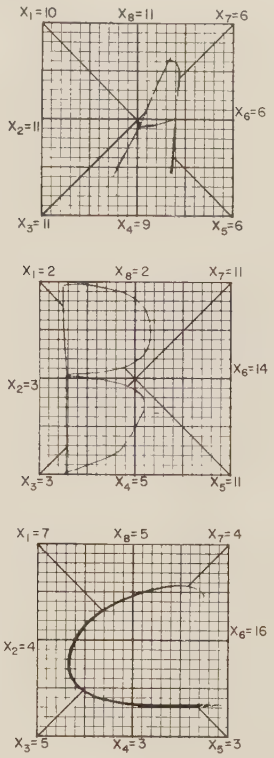

Fig. 3—Measurements made on the three examples of Fig. 1.

It should be emphasized that these particular measures were used, not because of any belief in their inherent value for letter-recognition, but merely because they were easy to obtain, and because there was some hope of their being approximately normally distributed.

Computations

No attempt was made to verify the assumptions of normality or of equality of covariance matrices before using the model.

First, the covariance matrix of the entire sample was computed. The results are given in Table I. Next, this matrix was inverted. The results are given in Table II.

The mean vectors for the three letters are given in Table III.

Lastly, the functions u_{ij} were computed and were found to be:

$$u_{AB} = 0.820X_1 - 0.175X_2 - 0.440X_3 + 0.419X_4 - 0.030X_5 + 0.048X_6 + 0.130X_7 - 0.034X_8 - 5.51$$

$$u_{AC} = 0.106X_1 + 0.046X_2 - 0.291X_3 + 0.344X_4 + 0.024X_5 - 0.343X_6 - 0.005X_7 + 0.084X_8 + 1.87$$

$$u_{BC} = -0.715X_1 + 0.220X_2 + 0.149X_3 - 0.074X_4 + 0.054X_5 - 0.391X_6 - 0.135X_7 + 0.118X_8 + 7.39$$

and, of course,

$$u_{BA} = -u_{AB}$$

$$u_{CA} = -u_{AC}$$

$$u_{CB} = -u_{BC}.$$

TABLE I

COVARIANCE MATRIX

2.748	2.265	1.218	2.230	− .783	−1.262	− .503	1.608
	3.277	1.719	1.887	−2.039	−4.329	−2.169	1.584
		3.172	− .608	.152	− .037	− .317	1.264
			8.214	−2.780	−4.817	−1.943	1.380
				14.459	10.603	10.605	.327
					19.333	11.569	.205
						14.445	.013
							3.725

TABLE II

COVARIANCE MATRIX INVERTED

1.384	−1.121	.042	− .240	.043	− .257	.023	− .036
	1.904	− .500	.098	− .024	.446	− .090	− .215
		.611	.103	− .011	− .102	.043	− .045
			.222	.010	.073	− .028	− .060
				.165	− .033	− .096	− .021
					.227	− .091	− .081
						.197	.037
							.419

TABLE III

MEAN VECTORS FOR THE LETTERS "A," "B," AND "C"

$\mu_A' =$	[7.72	6.66	4.72	8.32	5.86	7.02	7.70	4.14]
$\mu_B' =$	[5.62	5.82	5.76	3.56	5.94	7.20	6.30	3.20]
$\mu_C' =$	[6.36	4.54	5.52	3.28	10.36	15.42	12.22	3.54]

The 150 samples were then classified into A, B, C in accordance with the rule, (3), above.

Results

The results of this run are tabulated in Table IV. It will be seen that the recognition accuracy was 95 per cent.

An additional sample of 30 letters[9] which had not been used in the calculation of the recognition function was tested. Results are given in Table V. There was one error out of thirty.

Discussion

Exact interpretation of the illustrative example is difficult, since the example tests not only the excellence of the recognition function but also the excellence of the measures, that is, of the "receptor". Nonetheless, the results seem encouraging, in that good recognition accuracy was obtained despite the fact that the measures were not optimally chosen, that the assumptions of the model were assuredly violated to some extent, and that the sample size was small. The computations were readily performed on an LGP-30 computer and required only a small programming effort.

SOLUTION WITH NORMAL VARIABLES AND UNEQUAL COVARIANCE MATRICES

If we assume only that the variables are normally distributed and do not make the assumption of equal covariance matrices, we may proceed as follows.

[9] These samples were generated by 30 different people who had not contributed to the original sample.

TABLE IV

RESULTS OF FIRST RUN; RECOGNITION OF 150 SAMPLES

		Input A	Input B	Input C
Output	A	49	4	0
Output	B	1	45	1
Output	C	0	1	49

TABLE V

RESULTS OF SECOND RUN; RECOGNITION OF 30 ADDITIONAL SAMPLES NOT USED IN CALCULATING THE RECOGNITION FUNCTION

		Input A	Input B	Input C
Output	A	10	1	0
Output	B	0	9	0
Output	C	0	0	10

The probability density of X when X is from population π_i is

$$p_i(x) = \frac{1}{(2\pi)^{p/2} \mid V_i \mid^{1/2}} \exp\left[-1/2(x - \mu_i)' V_i^{-1}(x - \mu_i)\right]$$

The ratio of two densities is

$$\frac{p_i(x)}{p_j(x)} = k_{ij} \frac{\exp\left[-1/2(x - \mu_i)' V_i^{-1}(x - \mu_i)\right]}{\exp\left[-1/2(x - \mu_j)' V_j^{-1}(x - \mu_j)\right]}$$

where

$$k_{ij}^2 = \frac{\mid V_j \mid}{\mid V_i \mid} .$$

As before, we define

$$u_{ij} = \log \frac{p_i(X)}{p_j(X)} .$$

Substituting and rearranging terms we may write

$$u_{ij} = -\tfrac{1}{2} X'[V_i^{-1} - V_j^{-1}]X + X'[V_i^{-1}\mu_i - V_j^{-1}\mu_j]$$
$$- \tfrac{1}{2}\mu_i' V_i^{-1}\mu_i + \tfrac{1}{2}\mu_j' V_j^{-1}\mu_j + \log k_{ij}.$$

These functions are not linear function of X. If the mponents of X are $X_1, \ldots, X_p$, each of the above nctions is of the form

$$\sum_{\substack{u=1 \\ v=1}}^{p} a_{uv}X_uX_v + \sum_{u}^{p} b_uX_u + c.$$

This expression is a polynomial containing p^2+p+1 rms.

Thus, the resulting recognition function would be nsiderably more complicated than the one obtained der the equal-covariance-matrix assumption. More- er, the sampling-error problem looms larger. If, as fore, p is the number of measures and m is the number categories, the number of quantities to be estimated is equal to $mp+\frac{1}{2}m(p^2+p)$. If $m=p=10$, we are required to estimate 650 quantities. The resulting recognition functions will therefore approach the optimum at a slower rate (as sample size increases) than the recognition function found by the earlier model.

ACKNOWLEDGMENT

We would like to acknowledge indebtedness and to express thanks to our friend, Dr. J. E. Keith Smith, of the M.I.T. Lincoln Laboratory, who first pointed out to us the relevance to the problem at hand in the discussion given by T. W. Anderson and, of course, to Dr. Anderson, whose presentation seems to us to clarify significantly the handling of several mathematical problems in pattern recognition and signal detection.

The Simplification of Multiple-Output Switching Networks Composed of Unilateral Devices*

G. C. VANDLING†, MEMBER, IRE

Summary—The purpose of this paper is to show that two-level o more than two gates in cascade) multiple-output switching tworks composed of unilateral switching devices such as diodes n be simplified or minimized in much the same manner as single- tput networks.

This is accomplished by extending the notation and techniques ed in the simplification of two-level single-output switching net- rks to multiple-output switching networks. A simple procedure for entifying multiple-output prime implicants is devised and, as a al result, an algorithm is presented which can be used to mini- ze the switching network corresponding to a number (q) of given olean expressions of the same variables. This algorithm is based the Quine rules but has been modified to take advantage of the -called "don't care" conditions which occur because some inputs e forbidden or because some outputs are of no concern. This gorithm can readily be programmed on a digital computer if de- ed.

WHILE the general problem of minimizing a Boolean expression has not been solved, Quine and others have treated the problem of finding e simplest irredundant minterm- or maxterm-type olean expression.[1] These representations are of in- rest for a number of reasons. For example, a func- on so expressed is often much simpler than a given nction and can sometimes be further simplified algebraically. Also, either the simplest minterm-type or maxterm-type representation leads to a minimum diode count in two-level (no more than two gates in cascade) diode logic circuits.

Systems often require a great number of switching circuits, many of which may be described by Boolean functions of the same variables. When this occurs, circuit complexity and cost can often be reduced by using the logical output of one or more gates simultaneously in switching circuits represented by two or more Boolean functions. Such circuits are called multiple-output circuits; the general case consists of a switching circuit with n-inputs and q-outputs where there is no restriction on how many components may be shared. Such a circuit can be described by a number (q) of single-output Boolean functions. Simple single-output and multiple-output switching networks are illustrated in Fig. 1.

The purpose of this paper is first to extend the notation frequently used to describe n-input single-output networks to describe fully n-input q-output switching networks, of which the former is considered to be a special case. Having accomplished this, it will be shown that some techniques currently used to determine the simplest minterm- or maxterm-type single-output Boolean expression equivalent to a given expression may also be extended. These techniques may then be used to determine the simplest multiple-output expression equivalent to a number (q) of given single output Boolean expressions of the same variables. Such a repre-

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[1] Often called, respectively, disjunctive normal form and con- ctive normal form.

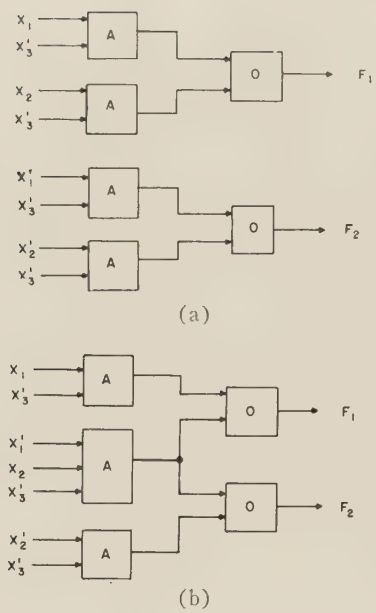


Fig. 1—(a) Two single-output switching circuits. (b) A multiple-output switching circuit which corresponds to the two switching circuits of (a).

sentation will lead to a minimum diode count in two-level multiple-output diode-logic circuits and is also amenable to further algebraic simplification. In general, such a representation cannot be realized by a series parallel combination of relay contacts.

I. Some Preliminary Matters of Notation

A single-output Boolean expression of the variables $X_1, X_2, \cdots, X_n$, involving the literals $X_1, X_1', X_2, X_2', \cdots, X_n, X_n'$, will be written $F_i(X_1, X_2, \cdots, X_n)$ where the subscript i is introduced for identification. Any conjunction of literals is called a term. The single-output minterm (or sum-of-products canonical or full disjunctive normal) representation of F_i is

$$F_i = \sum_{j=0}^{2^n-1} Z_{i,j} f_j, \qquad Z_{i,j} = 0, 1 \tag{1}$$

where each f_j is called a minterm and $\sum$ denotes logical summation (disjunction). Every f_j corresponds to one of the 2^n terms formed from the conjunction of each variable or its complement with every other variable or its complement. The subscript j of $f_j(X_1, X_2, \cdots, X_n)$ is defined by the *arithmetic sum*

$$i = b_1 + 2b_2 + 4b_3 + \cdots + 2^{n-1}b_n$$

where $b_p = 1$ if X_p appears in the product f_j and $b_p = 0$ if X_p' appears. The $Z_{i,j}$'s are assigned the values 1 or 0 depending on whether or not the device or network to be described by F_i is to have a 1 or 0 output for the combination of input values represented by f_j. By appropriately assigning the $Z_{i,j}$'s, any one of the 2^{2^n} switching functions of n variables may be represented.

A term θ is said to subsume a term ϕ if every literal appearing in ϕ appears in θ and if no variable appears both complemented and uncomplemented in either term. Often, Boolean expressions may be simplified by the application of the identity

$$X_1 = X_1X_2 + X_1X_2'.$$

Here, both X_1X_2 and X_1X_2' subsume X_1. A minterm-type expression is any sum-of-products Boolean expression. Each term may or may not be a minterm. A sum-of-products canonical expansion is considered to be a special case of minterm-type expression and is often called a minterm expansion.

A term θ is called a prime implicant of F_i if θ implies F_i and if θ subsumes no other term containing fewer literals which implies F_i. Quine has shown that a minimal irredundant minterm-type Boolean function equivalent to F_i is a sum of prime implicants of F_i.[2]

Any function of the variables $X_1, X_2, \cdots, X_n$, such as H_i will be said to be equivalent to a given function of the same variables, F_i, if, and only if, for every possible combination of input values the logical values of F_i and H_i are the same.

An irredundant minimal sum-of-products expression equivalent to some given sum-of-products canonical expression may always be obtained by the repeated application of just two Boolean identities:

$$\beta_1\beta_2 + \beta_1\beta_2' = \beta_1$$

$$\beta_1 + \beta_1 = \beta_1$$

in addition to the commutative laws. Here, β represents a literal or conjunction of literals. More satisfactory systematic simplification techniques have been developed by Aiken, Quine, Karnaugh, Veitch and others.[3–6]

II. Multiple Output Switching Networks

It is desirable to devise a notation for multiple-output switching networks which, in addition to describing the network, makes possible the complete identification of each output function and which is reducible to the familiar minterm or minterm-type expression for the special case of one output.

Given q different single-output functions of n variables, each of which is expressed in minterm form as

$$F_i = \sum_{j=0}^{2^n-1} Z_{i,j} f_j \qquad Z_{i,j} = 0, 1; \; i = 1, 2, \cdots, q$$

[2] W. V. Quine, "The problem of simplifying truth functions," *Am. Math. Monthly*, vol. 59, pp. 521–531; October, 1952.

[3] Staff of Harvard Computational Lab., "Synthesis of Electronic Computing and Control Circuits," Harvard University Press, Cambridge, Mass.; 1951.

[4] W. V. Quine, "A way to simplify truth functions," *Am. Math. Monthly*, vol. 62, pp. 627–631; November, 1955.

[5] M. Karnaugh, "The map method for synthesis of combinational logic circuits," *Commun. and Electronics* (*Trans. AIEE*, pt. 1, v 72), pp. 593–599; November, 1953.

[6] E. W. Veitch, "A chart method for simplifying truth functions," *Proc. Assoc. Computing Machinery Conf.*, Pittsburgh, Pa., May 2 1952; pp. 127–133.

consider the set S_j composed of all possible $P_{k,j}$'s ined as follows:

$$P_{k,j} = \sum_{i=1}^{q} Z_{i,j} f_j \tag{5}$$

ere $Z_{i,j}$ can be either a zero or a one and where the bscript k is given by *the arithmetic sum*

$$k = Z_{1,j} + 2Z_{2,j} + 4Z_{3,j} + \cdots + 2^{q-1}Z_{q,j}.$$

Theorem 1: Set S_j contains 2^q members.

Proof: The proof of this theorem is apparent, since, the equation defining the k's, each $P_{k,j}$ corresponds one ordered combination of the f_j's.

Since there are 2^q possible $P_{k,j}$'s for any j, and since ere are 2^n minterms, it follows that there are $(2^q)^{2^n}$ itching functions for an n-input q-output network ere $q = 1, 2, 3, \cdots$. This is the number of combinans of 2^n things (minterms) each of which can be disbuted in 2^q ways between the q functions describing individual outputs. Any notation devised must, erefore, be capable of completely describing any of the $)^{2^n}$ switching functions. The P's are expressible in olean form.

Theorem 2: If the P's are expressed as two valued riables, no less than q auxiliary variables are required.

Proof: The proof follows from recognizing that S_j conns 2^q members. Clearly, no less than a number (q) of o valued variables can be used to identify 2^q condins.

In order to express the $P_{k,j}$'s in Boolean form we induce the two valued variables $y_1, y_2, \cdots, y_q$. These xiliary variables will be made subject to additional strictions. By expressing the P's as a function of the xiliary variables $y_1, y_2 \cdots y_q$, any multiple-output pression can be completely and unambiguously deibed by

$$\mathfrak{F} = \sum_{i=1}^{q} \sum_{j=0}^{2^n-1} y_i Z_{i,j} f_j \tag{6}$$

ere $Z_{i,j} = 1$ if f_j is in F_i and 0 otherwise. We introduce is as the definition of the minterm canonic form for a ltiple-output network. Each $y_i f_j$ is a multiple-output nterm (mom).

The following example illustrates this notation. Conler the following three functions of two variables:

$$F_1 = X_1X_2 + X_1'X_2'$$
$$F_2 = X_1'X_2' + X_1'X_2$$
$$F_3 = X_1X_2 + X_1X_2'.$$

ese three single-output functions can be combined o one multiple-output function,

$$\mathfrak{F} = y_1X_1X_2 + y_1X_1'X_2' + y_2X_1'X_2' + y_2X_1'X_2 + y_3X_1X_2 + y_3X_1X_2'.$$

becomes F_1 when $y_1 = 1$, $y_2 = y_3 = 0$ are substituted in e above equation, and, similarly, F_2 and F_3 can be obtained. Note that each term of $\mathfrak{F}$ can be placed in one-to-one correspondence with a term in one of the single-output networks. Thus $y_1X_1'X_2'$ corresponds to $X_1'X_2'$ in function F_1. Since when $q = 1$, $y_1 = 1$, and $y_2 = y_3 = 0$, (6) reduces to the minterm canonical form for a single-output network F_1, such a network is considered to be a special case of the more general type of an n-input q-output network.

A function

$$\mathfrak{F}(y_1, y_2, \cdots, y_q, X_1, X_2, \cdots, X_n),$$

will be said to be equivalent to a given function

$$\mathfrak{H}(y_1, y_2, \cdots, y_q, X_1, X_2, \cdots, X_n)$$

if, for every possible assignment of zeros and ones to the input variables (X's) and every assignment of the y's according to the following convention, H_i has the same logical value (zero or one) as F_i. This convention is that when $y_i = 1$ then $y_1 = y_2 = \cdots = y_{i-1} = y_{i+1} = \cdots = y_q = 0$. Equivalence of multiple-output Boolean functions therefore actually requires simultaneous equivalence of all the corresponding single-output circuits. The equivalence of single-output Boolean functions has previously been defined.

Since the auxiliary variables y_i are two valued, function $\mathfrak{F}$ obeys many of the laws of Boolean algebra. Terms may be combined algebraically transforming function $\mathfrak{F}$ into any equivalent multiple-output circuit.

Three rules of combination are given below:

$$\alpha_1\beta_1 + \alpha_1\beta_1 = \alpha_1\beta_1 \tag{7}$$
$$\alpha_1\beta_1 + \alpha_2\beta_1 = (\alpha_1 + \alpha_2)\beta_1, \tag{8}$$
$$\alpha_1\beta_1\beta_2 + \alpha_1\beta_1\beta_2' = \alpha_1\beta_1. \tag{9}$$

Here, α represents an auxiliary variable or group of auxiliary variables of the form $(y_{1i} + y_{2i} + \cdots)$, while β represents a literal or conjunction of literals. The interpretation of these terms is of importance. The meaning of a specific term $y_1X_1X_2$, for example, is that "a gate corresponding to X_1X_2 can be used in output 1." A term $(y_1 + y_2)X_1X_2$ then means "a gate corresponding to X_1X_2 can be shared between outputs 1 and 2." From this interpretation it is apparent that $\cdots y_i + y_i \cdots$ is redundant and may conveniently be changed to y_i if it ever occurs in a term $\alpha\beta$. Except that terms are always written in the form $\alpha\beta$ for convenience, the rules of combination are commutative. It should be apparent that the use of these rules will not affect multiple-output equivalence as previously defined.

Only the three additional operations above have been defined and only these will be used in this paper. Although, for example, $\alpha_1\beta_1\beta_2 + \alpha_2\beta_1\beta_3 = \beta_1(\alpha_1\beta_2 + \alpha_2\beta_3)$ seems plausible, it is undefined and not used because it is not useful. While the operation

$$\alpha_1\beta_1\beta_2 + \alpha_1\beta_1\beta_3 = \alpha_1[\beta_1(\beta_2 + \beta_3)] \tag{10}$$

is useful, it leads to results other than sum-of-products and will not be considered in this paper. The auxiliary

variables are ignored when deciding whether or not a multiple-output function is sum-of-products.

For multiple-output relationships a term θ is said to subsume a term ϕ if

1) Every literal appearing in ϕ appears in θ, and if no variable appears both complemented and uncomplemented in either term, while
2) Every auxiliary variable appearing in θ appears in ϕ.

For example, $y_1X_1X_2$ subsumes y_1X_1, $y_2X_1X_2$ subsumes $(y_1+y_2)X_1$, and $(y_1+y_2)X_1X_2$ subsumes $(y_1+y_2+y_3)X_1X_2$. A term ϕ is not necessarily more desirable than a term θ which subsumes it. For example, while $(y_1+y_2+y_3)X_1X_2$ is subsumed by $(y_1+y_2)X_1X_2$, it would require five diodes in a diode realization (two diodes for the gate X_1X_2 and one in each of the output OR gates for F_1, F_2, and F_3), while $(y_1+y_2)X_1X_2$ would require four. While it is obvious that both of these terms would not be required, additional information is required if the choice between them is not to be arbitrary. This fact illustrates an additional complication encountered in the simplification of multiple-output networks.

The rules of combination defined above are analogous to (3) and (4) for single-output networks. These rules—together with the knowledge that they are commutative—can be used to obtain the simplest sum-of-products multiple-output expression equivalent to a given $\mathfrak{F}$. In any but the simplest cases, however, this will require an exhaustive search. A more satisfactory procedure will be presented subsequently.

As with single-output expressions, there exists a dual- or maxterm-type multiple-output representation for which a notation could be devised if desired. Such a representation will not be treated here, since the dual network can readily be found as will subsequently be shown by example.

It must be emphasized that despite the fact that n variables and q auxiliary variables are used to represent a multiple output network, the problem of minimizing a multiple-output network *is not* equivalent to minimizing an $n+q$ variable single-output Boolean network. This is so because of the additional constraints placed on the auxiliary variables. This is best appreciated by noticing that although $\mathfrak{F}$ resembles an $n+q$ variable single-output switching function, no y_i' terms appear. This is a distinctive feature of our multiple-output notation. It is also of interest to note that there are $(2^q)^{2^n}$ switching functions for an n-input q-output switching function and $(2)^{2^{n+q}}$ switching functions for an $n+q$ variable switching network, and that

$$2^{2^{n+q}} = 2^{2^n 2^q} = (2^{2^q})^{2^n} \gg (2^q)^{2^n} \quad \text{for } q = 2, 3, \cdots.$$

It is, therefore, also obvious that the switching functions of an $n+q$ input, single-output network cannot be placed in one-to-one correspondence with the switching functions of an n-input q-output multiple-output network.

III. Prime Implicants of Multiple Output Functions

In this section we define prime implicants for multiple-output functions which are analogous to prime implicants for single-output functions. Since, as has been previously explained, single-output functions are considered a special case of multiple-output functions, prime implicants of single-output functions are special cases of the more general multiple-output prime implicants.

We first define 2^q-1 functions G_m, each of which corresponds to a subset of the set of all minterms appearing in the q functions F_i:[7]

$$\begin{aligned}
G_1 &= F_1 \\
G_2 &= F_2 \\
G_3 &= F_1 \cap F_2 \\
G_4 &= F_3 \\
G_5 &= F_1 \cap F_3 \\
G_6 &= F_2 \cap F_3 \\
G_7 &= F_1 \cap F_2 \cap F_3 \\
&\vdots \\
G_{2^q-1} &= F_1 \cap F_2 \cap F_3 \cap \cdots \cap F_q.
\end{aligned}$$

The subscripts m are assigned by the following arithmetic sum:

$$m = w_1 + 2w_2 + 4w_3 + \cdots + 2^{i-1}w_i + \cdots + 2^{q-1}w$$

where $w_i = 1$ if G_m is a function of F_i and zero otherwise. Conversely, we know that $G_{15} = F_1 \cap F_2 \cap F_3 \cap F_4$ since $m = 15 = 1+2+4+8$, $w_1 = w_2 = w_3 = w_4 = 1$. Any given minterm can occur in one, more than one, or all of the functions G_m. Throughout this paper $F_1, F_2, \cdots, F_q$ and $\mathfrak{F}$ are considered to be expressed in single-output minterm form and multiple-output minterm form respectively. This we can do without loss of generality since any minterm-type expression is easily expanded to canonical form. For completeness, we also define $G_0 = F_1' \cap F_2' \cap F_3' \cap \cdots \cap F_q'$ in addition to the above. The symbol F_i' denotes the complement of F_i and F_i' contains all those minterms not contained in F_i for a given n. This is of little interest in the simplification of minterm-type Boolean functions.

We now consider all the related single-output minterms $g_{m,j}$ which occur in the single-output expressions $G_1, G_2, G_3, \cdots, G_{2^q-1}$. For each single-output prime implicant (sopi) of G_m, $P_r(g_{m,j})$, containing $g_{m,j}$, there is a corresponding multiple-output prime implicant (mopi) of $\mathfrak{F}$. By definition, this mopi is

$$K(y_1, y_2 \cdots y_i \cdots y_q) P_r(g_{m,j}),$$

[7] The symbol $\cap$ is used to identify an operation on functions. $F_2 \cap F_3$ is a disjunction of all minterms common to F_2 and F_3. $F_1 \cap F_2 \cap F_3$ is a disjunction of all minterms common to F_1, F_2, and F_3, and so on.

here

$(y_1, y_2, \cdots y_i \cdots y_q) P_r(g_{m,j})$

$(h_1y_1 + h_2y_2 + \cdots + h_iy_i + \cdots + h_qy_q) P_r(g_{m,j})$ (11)

d where $h_i = 1$ if G_m is a function of F_i and 0 otherwise. etwork-wise, the multiple-output prime implicants ay be interpreted as those corresponding to shared tes—$m \neq 0, 1, 2, 4, \cdots, 2^{q-1}$ and those correspond- g to unshared gates ($m = 1, 2, 4, \cdots, 2^{q-1}$). If a min- rm y_if_j subsumes only one prime implicant $P_r(g_{m,j})$ is prime implicant is called an *essential term* and must ppear as a term in the simplest irredundant multiple- utput function.

A multiple-output minterm-type expression $\mathcal{K}$ is redundant if it cannot be transformed into an expres- on $\mathcal{G}$, which is its equivalent, by deleting one or more rms or literals. The process of transforming a re- undant expression into an equivalent expression by eleting literals and/or terms is called *simplification.*

Many criteria have been used previously to define he minimum or simplest irredundant minterm-type ngle-output expression equivalent to some given ex- ression. Among these are:

1) $\mathcal{G}$ is simpler than $\mathcal{K}$ if it contains fewer terms than $\mathcal{K}$.
2) $\mathcal{G}$ is simpler than $\mathcal{K}$ if the circuit required to realize it requires fewer diodes than does the circuit required to realize $\mathcal{K}$.
3) $\mathcal{G}$ is simpler than $\mathcal{K}$ if it contains fewer literals than $\mathcal{K}$.

ny of these criteria can be applied to multiple-output xpressions as well. The auxiliary variables, however, re not counted as literals.

Having introduced multiple-output prime implicants nd essential terms, we prove the following theorem.

Theorem 3: The simplest minterm-type multiple-out- ut expression $\mathcal{K}$ equivalent to some given expression $\mathcal{F}$ a disjunction of the multiple-output prime implicants.

Proof: Assume that $\mathcal{K}$ contains a term μ which is not multiple-output prime implicant of $\mathcal{F}$. If μ is not a ultiple-output prime implicant of $\mathcal{F}$, $'\mu$ (μ less its auxil- ry variables) is not a prime implicant of its associated unction G by definition. If $'\mu$ is not a prime implicant f G, one or more literals may be deleted from it trans- rming it into a prime implicant $'\psi$ of G. The corres- onding multiple-output prime implicant ψ now con- ains fewer literals than μ and hence, if it is substituted or μ, the resulting expression is now simpler than $\mathcal{K}$ in oth sense 2) and 3) above. This, however, contradicts ur assumption that $\mathcal{K}$ is the simplest possible multiple- utput expression, thereby proving the theorem.

IV. Simplification of Multiple-Output Expressions

The analogy between single-output and multiple- utput expressions is complete. One solution to the gen- ral problem of finding the simplest irredundant min- term-type representation of a specified function—either single-output or multiple-output—consists of:

1) Determining all the prime implicants (multiple-output prime implicants) of the specified Boolean function.
2) Identifying all the essential prime implicants (essential multiple-output prime implicants).
3) Selecting from the group of nonessential prime implicants (multiple-output prime implicants) the simplest set which includes all minterms which do not subsume essential prime implicants. The disjunction of these terms with the essential terms will result in the simplest possible equivalent minterm-type expression (multiple output minterm-type expression).

Essentially, this is an outline of the procedure suggested by Quine. More specifically, for multiple-output prime implicants, step 1) can consist of:

a) Identifying the auxiliary functions G_m.
b) Finding all the single-output prime implicants of all the functions G_m.
c) Converting each of these single-output prime implicants $P_r(g_{m,j})$ into multiple-output prime implicants.

The functions F_i will usually be known or can easily be determined. The functions G_m can be calculated from their defining equations using matrix techniques or some alternate method.[8] Any of the well-known techniques presently used to determine the prime implicants of single-output expressions can be used to determine all the prime implicants of each 2^{q-1} functions G_m, for example, one of the map methods or the method of Quine as adapted by McCluskey.[5,6,9] These single-output prime implicants $[P_r(g_{m,j})]$ can then be transformed into the corresponding mopi as discussed previously. For multiple-output functions, steps 2 and 3 are nearly equivalent to those used for single-output expressions. This will be made clear in the following examples.

Example 1: Using the least diode count as a criterion for minimality, find the simplest two-level realization of the following output functions:

$$F_1 = G_1 = X_1X_2X_3' + X_1X_2'X_3 + X_1'X_2X_3' + X_1'X_2'X_3'$$

$$F_2 = G_2 = X_1X_2'X_3' + X_1X_2X_3 + X_1'X_2X_3' + X_1'X_2'X_3'$$

$$F_3 = G_4 = X_1X_2X_3 + X_1X_2'X_3' + X_1X_2'X_3.$$

Part I: We will first find the minimum multiple-output minterm-type expression equivalent to the given outputs and we begin by constructing the auxiliary functions.

[8] E. J. Schubert, "Matrix analysis of logical networks," *Commun. and Electronics* (*Trans. AIEE*, pt. 1, vol. 77) pp. 10–13; March, 1958.
[9] E. J. McCluskey, Jr., "Minimization of Boolean functions," *Bell Sys. Tech. J.*, vol. 35, pp. 1417–1444; November, 1956.

$$G_3 = F_1 \cap F_2 = X_1'X_2X_3' + X_1'X_2'X_3'$$
$$G_5 = F_1 \cap F_3 = X_1X_2'X_3$$
$$G_6 = F_2 \cap F_3 = X_1X_2X_3 + X_1X_2'X_3'$$
$$G_7 = F_1 \cap F_2 \cap F_3 = 0.$$

The prime implicants of the output functions and the auxiliary functions are listed in Table I along with the corresponding multiple-output prime implicants. In Table II, each minterm is associated with the prime implicants it subsumes. Since only one check mark appears in the column labeled $y_1X_1X_2X_3'$, $y_1X_2X_3'$ is an *essential term* and must appear in any minimal expression. The row corresponding to $y_1X_2X_3'$ and the columns corresponding to $y_1X_1X_2X_3'$ and $y_1X_1'X_2X_3'$ may therefore be deleted. From Table II a revised table (Table III) listing the nonessential mopi and their associated minterms may be constructed. An exhaustive examination of this table will show that the function

$$\mathcal{G} = y_1X_2X_3' + (y_1 + y_2)X_1'X_3' + (y_1 + y_3)X_1X_2'X_3 + (y_2 + y_3)X_1X_2X_3 + (y_2 + y_3)X_1X_2'X_3'$$

requires only 22 diodes and leads to a minimal two-level AND-OR representation of the given functions. The resulting network configuration is shown in Fig. 2.

Part II: We will now find the minimum OR-AND representation of the given functions. Although a multiple-output maxterm-type notation could be devised to aid us if desired, it is more convenient to find the simplest AND-OR representation of $\mathcal{F}'$ and construct the dual network for $\mathcal{F}$. Complementing the given expression we have:

$$F_1' = G_1' = X_1X_2'X_3' + X_1X_2X_3 + X_1'X_2X_3 + X_1'X_2'X_3$$
$$F_2' = G_2' = X_1X_2X_3' + X_1X_2'X_3 + X_1'X_2X_3 + X_1'X_2'X_3$$
$$F_3' = G_4' = X_1X_2X_3' + X_1'X_2X_3 + X_1'X_2'X_3 + X_1'X_2X_3' + X_1'X_2'X_3'.$$

The auxiliary functions are:

$$G_3' = F_1' \cap F_2' = X_1'X_2X_3 + X_1'X_2'X_3$$
$$G_5' = F_1' \cap F_3' = X_1'X_2'X_3 + X_1'X_2X_3$$
$$G_6' = F_2' \cap F_3' = X_1X_2X_3' + X_1'X_2X_3 + X_1'X_2'X_3$$
$$G_7' = F_1' \cap F_2' \cap F_3' = X_1'X_2X_3 + X_1'X_2'X_3.$$

The prime implicants of all the output functions and auxiliary functions are listed in Table IV (p. 484) along with their associated mopi. Tables V and VI are constructed as previously. Again, by exhaustive examination, the minimal expression is found to be:

$$\mathcal{G}' = y_3X_1' + y_1X_2X_3 + y_1X_1X_2'X_3' + y_2X_2'X_3 + (y_2 + y_3)X_1X_2X_3' + (y_1 + y_2)X_1'X_3.$$

Its dual network requires 20 diodes and is shown in Fig. 3.

V. Incomplete Truth Functions

We will now discuss the problem of simultaneously minimizing a set of incompletely specified single-output truth functions. Truth functions are incompletely specified when so-called "don't care" conditions exist. These "don't care" conditions occur either because some input are forbidden or because for some inputs the output is of no concern. That "don't cares" can be used to reduce the complexity of switching circuits is well known and will not be discussed again here.[10,11]

It is assumed that we are given, to simplify, q Boolean expressions $F_1, F_2, \cdots, F_q$, each of which is expressed as a sum of minterms, some of which are identifiable as "don't cares." Each individual expression F_i may or may not contain "don't cares." For example, one such expression might be

$$F_i = X_1'X_2X_3X_4' + X_1'X_2'X_3X_4 + Z_{1,1}X_1'X_2'X_3'X_4 + Z_{1,0}X_1'X_2'X_3'X_4'.$$

We are justified in making this assumption since any problem statement which is neither incomplete nor contradictory may be restated in this manner. The Z's are appended to the "don't care" minterms and may be assigned the value of either zero or one as is necessary to achieve the most desirable simplification. The other minterms are called *required minterms* and each corresponding multiple-output minterm *must always subsume at least one mopi appearing in any minimal expression.*

We now restate the Quine rules so that they may apply to the q incomplete truth functions.[12]

1) First assign each Z (one is associated with every "don't care" minterm) the value one. That this has been done is assumed throughout the remaining steps.
   a) Identify the auxiliary functions G_m.
   b) Find all the single-output prime implicants of all the functions G_m.[13]
   c) Convert each of the above single-output prime implicants into mopi.
2) Prepare a prime implicant table. There will be one row for each mopi found in step 1-c above and there will be one column for each of the *required minterms.* Identify each row with a mopi and each column with a required multiple-output minterm.

[10] M. Phister, Jr., "Logical Design of Digital Computers," John Wiley and Sons, Inc., New York, N. Y., pp. 97–106; 1958.

[11] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y., ch. 5; 1958.

[12] This procedure is analogous to a procedure which can be used to simplify single-output Boolean expressions containing don't cares. (Phister, *op. cit.*, p. 98).

[13] If map methods are used to determine the prime implicants, the prime implicants of the functions F_i are found by conventional methods (the Z's are assigned as necessary for this part). (Phister, *op. cit.*, pp. 102–105.) However, all the Z's are still assigned the value one before the functions G_m are determined.

TABLE I

List of Prime Implicants for Example 1

Prime Implicants	Corresponding Mopi
F_1: $x_2\,x_3'$	$y_1\,x_2\,x_3'$
$x_1'\,x_3'$	$y_1\,x_1'\,x_3'$
$x_1\,x_2'\,x_3$	$y_1\,x_2'\,x_3$
F_2: $x_2'\,x_3'$	$y_2\,x_2'\,x_3'$
$x_1'\,x_3'$	$y_2\,x_1'\,x_3'$
$x_1\,x_2\,x_3$	$y_2\,x_1\,x_2\,x_3$
F_3: $x_1\,x_3$	$y_3\,x_1\,x_3$
$x_1\,x_2'$	$y_3\,x_1\,x_2'$
G_3: $x_1'\,x_3'$	$(y_1 + y_2)\,x_1'\,x_3'$
G_5: $x_1\,x_2'\,x_3$	$(y_1 + y_3)\,x_1\,x_2'\,x_3$
G_6: $x_1\,x_2\,x_3$	$(y_2 + y_3)\,x_1\,x_2\,x_3$
$x_1\,x_2'\,x_3'$	$(y_2 + y_3)\,x_1\,x_2'\,x_3'$
G_7: ---	---

TABLE II

Table of Prime Implicants for Example 1

MOPI \ MOM	$y_1\,x_1\,x_2'\,x_3'$	$y_1\,x_1\,x_2'\,x_3$	$y_1\,x_1'\,x_2\,x_3'$	$y_1\,x_1'\,x_2'\,x_3'$	$y_2\,x_1\,x_2'\,x_3'$	$y_2\,x_1\,x_2\,x_3$	$y_2\,x_1'\,x_2'\,x_3'$	$y_2\,x_1'\,x_2\,x_3$	$y_3\,x_1\,x_2\,x_3$	$y_3\,x_1\,x_2'\,x_3'$	$y_3\,x_1'\,x_2\,x_3$
$y_1\,x_2\,x_3'$	✓		✓								
$y_1\,x_1'\,x_3'$			✓	✓							
$y_1\,x_1\,x_2'\,x_3$		✓									
$y_2\,x_2'\,x_3'$					✓		✓				
$y_2\,x_1'\,x_3'$							✓	✓			
$y_2\,x_1\,x_2\,x_3$						✓					
$y_3\,x_1\,x_3$									✓		✓
$y_3\,x_1\,x_2'$										✓	✓
$(y_1 + y_2)\,x_1'\,x_3'$			✓	✓			✓	✓			
$(y_1 + y_3)\,x_1\,x_2'\,x_3$		✓									✓
$(y_2 + y_3)\,x_1\,x_2\,x_3$						✓			✓		
$(y_2 + y_3)\,x_1\,x_2'\,x_3'$					✓					✓	
Essential Mopi: $y_1x_2x_3'$											

TABLE III

Revised Table of Prime Implicants for Example 1

MOPI \ MOM	$y_1\,x_1\,x_2'\,x_3$	$y_1\,x_1'\,x_2'\,x_3'$	$y_2\,x_1\,x_2'\,x_3'$	$y_2\,x_1\,x_2\,x_3$	$y_2\,x_1'\,x_2\,x_3'$	$y_2\,x_1'\,x_2'\,x_3'$	$y_3\,x_1\,x_2\,x_3$	$y_3\,x_1'\,x_2'\,x_3'$	$y_3\,x_1'\,x_2'\,x_3$	WEIGHT (DIODES REQUIRED)
$y_1\,x_1'\,x_3'$		✓								3
$y_1\,x_1\,x_2'\,x_3$	✓									4
$y_2\,x_2'\,x_3'$			✓			✓				3
$y_2\,x_1'\,x_3'$					✓	✓				3
$y_2\,x_1\,x_2\,x_3$				✓						4
$y_3\,x_1\,x_3$							✓		✓	3
$y_3\,x_1\,x_2'$								✓	✓	3
✓$(y_1 + y_2)\,x_1'\,x_3'$		⊘			⊘	⊘				4
✓$(y_1 + y_3)\,x_1\,x_2'\,x_3$	⊘								⊘	5
✓$(y_2 + y_3)\,x_1\,x_2\,x_3$				⊘			⊘			5
✓$(y_2 + y_3)\,x_1\,x_2'\,x_3'$			⊘					⊘		5

The check marks designate the nonessential mopi selected.
The circles denote the multiple-output minterms which subsume these mopi.

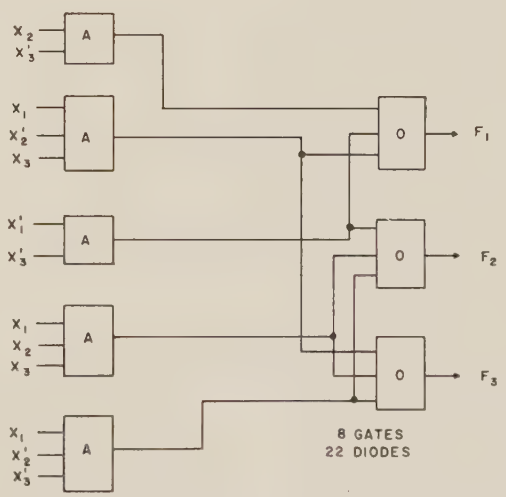


Fig. 2—Minimal AND/OR network representation for example 1, part 1.

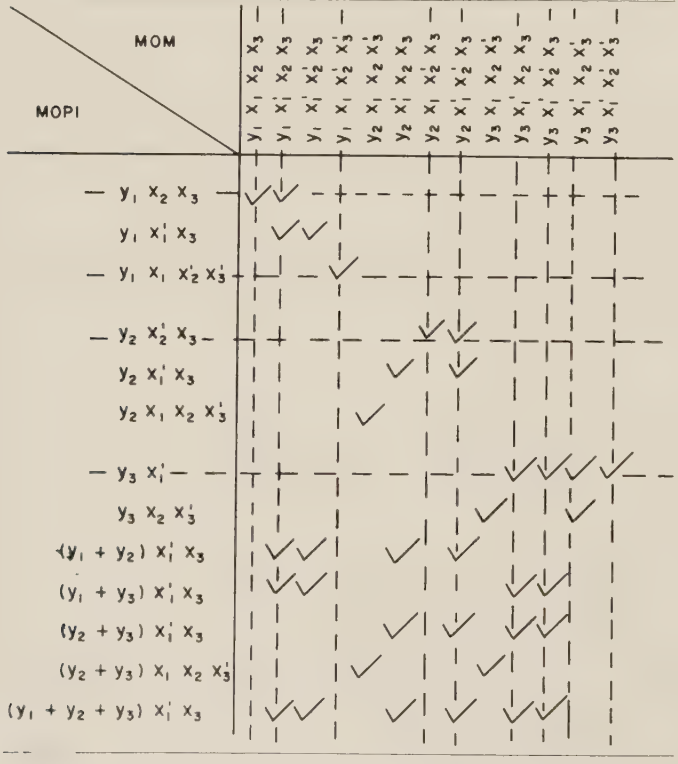
TABLE IV

List of Prime Implicants for Example 1, Part II

Prime Implicants	Corresponding Mopi
$\overline{F}_1$: $x_2\ x_3$	$y_1\ x_2\ x_3$
$x_1'\ x_3$	$y_1\ x_1'\ x_3$
$x_1\ x_2'\ x_3'$	$y_1\ x_1\ x_2'\ x_3'$
$\overline{F}_2$: $x_2'\ x_3$	$y_2\ x_2'\ x_3$
$x_1'\ x_3$	$y_2\ x_1'\ x_3$
$x_1\ x_2\ x_3'$	$y_2\ x_1\ x_2\ x_3'$
$\overline{F}_3$: x_1'	$y_3\ x_1'$
$x_2\ x_3'$	$y_3\ x_2\ x_3'$
$\overline{G}_3$: $x_1'\ x_3$	$(y_1 + y_2)\ x_1'\ x_3$
$\overline{G}_5$: $x_1'\ x_3$	$(y_1 + y_3)\ x_1'\ x_3$
$\overline{G}_6$: $x_1'\ x_3$	$(y_2 + y_3)\ x_1'\ x_3$
$x_1\ x_2\ x_3'$	$(y_2 + y_3)\ x_1\ x_2\ x_3'$
$\overline{G}_7$: $x_1'\ x_3$	$(y_1 + y_2 + y_3)\ x_1'\ x_3$

TABLE V

Table of Prime Implicants for Example 1, Part II



Essential mopi: $y_1x_2x_3$, $y_2x_2'x_3$, y_3x_1' and $y_1x_1x_2'x_3'$

TABLE VI

Revised Table of Prime Implicants for Example 1, Part

MOPI \ MOM	$y_1\ x_1'\ x_2'\ x_3$	$y_2\ x_1\ x_2\ x_3'$	$y_2\ x_1'\ x_2\ x_3$	$y_3\ x_1\ x_2'\ x_3'$	WEIGHT (DIODES REQUIRED)
$y_1\ x_1'\ x_3$	✓				3
$y_2\ x_1'\ x_3$			✓		3
$y_2\ x_1\ x_2\ x_3'$		✓			4
$y_3\ x_2\ x_3'$				✓	3
✓ $(y_1 + y_2)\ x_1'\ x_3$	⊘		⊘		4
$(y_1 + y_3)\ x_1'\ x_3$	✓				4
$(y_2 + y_3)\ x_1'\ x_2$			✓		4
✓ $(y_2 + y_3)\ x_1\ x_2\ x_3'$		⊘		⊘	5
$(Y_1 + y_2 + y_3)\ x_1'\ x_3$	✓		✓		5

The check marks designate the nonessential mopi selected. Th circles denote the multiple-output minterms which subsume the mopi.

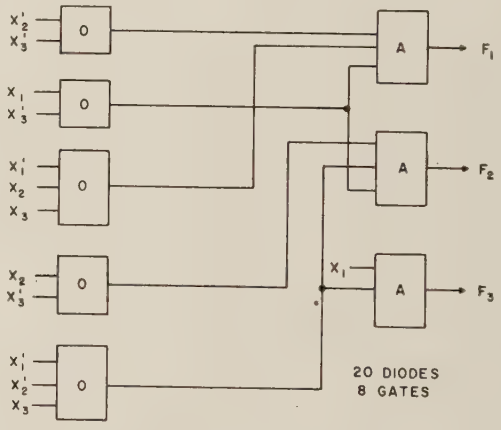


Fig. 3—Dual network for example 1, part 2, minimal OR/AND configuration.

(If f_j is a required minterm for output i, then $y_i f_j$ is the corresponding required multiple-output minterm.) There will be one multiple-output minterm for each required minterm in each of the q given expressions. "*Don't care*" *minterms never appear as column headings.* Place a check mark at the junction of the ith row and jth column if the ith prime implicant is subsumed by the jth minterm.

a) Delete any rows in which no check marks appear. (These prime implicants are subsumed only by "don't cares" and are unnecessary.)

b) Next, each column is examined.
   i) If only one check mark appears in a column, the mopi corresponding to the row in which it appears in is an *essential* mopi. Record all essential mopi.
   ii) All rows corresponding to essential mopi and all columns corresponding to mom which subsume essential mopi should be deleted.

c) If there are two rows i_a and i_b so that for *each* check mark appearing in row i_a, there appears a check mark in the corresponding column of row i_b,
   i) If the mopi corresponding to row i_b is more desirable than the mopi corresponding to row i_a—perhaps it requires fewer diodes to implement—then row i_a can be deleted from the prime implicant table.
   ii) If the mopi corresponding to row i_b is just as desirable as the mopi corresponding to row i_a—perhaps it requires the same number of diodes—then row i_a can be deleted from the prime implicant table *if all the minimal expressions are not required.*

d) If there are two columns j_a and j_b so that for *each* check mark appearing in column j_a there appears a check mark in the corresponding row of j_b, then column j_a may be deleted from the prime implicant table.

e) A revised prime implicant table can be constructed by omitting those rows and columns deleted in previous steps.

3) Examine the revised prime implicant table and select the simplest set of nonessential mopi which, when taken together, include at least one check mark in every column. The disjunction of these nonessential mopi with the essential mopi, found in step 2)-b), forms the simplest possible multiple-output minterm-type expression equivalent to the q given expression.

The prime implicant table constructed in step 2) displays the information we have obtained about each mopi and essential prime implicant in such a manner that certain relationships may readily be discerned. These relationships are in turn used to reduce the prime implicant table, thereby simplifying the exhaustive search ultimately required by step 3). Even this search, however, can be accomplished systematically by using a technique described by Petrick.[14]

Since we do not initially know how to best assign the "don't cares," we first assign each Z associated with a "don't care" minterm the value one, and thereby consider all possible ways they can be used to form mopi in steps 1)-b) and 1)-c). Some of the resulting terms are not useful because they are subsumed only by "don't care" minterms. These are readily identified and eliminated in step 2)-a) since only required minterms are used as column headings.

Step 2)-b)-i) follows directly from the definition of an essential term. Since each essential term will appear in any minimal solution, all mom which subsume essential terms have been accounted for and their respective columns may be deleted from the prime implicant table in step 2)-b)-ii).

Step 2)-c)-i) is used to eliminate mopi which imply simpler mopi for every assignment of variables and auxiliary variables for which a required mom, not subsuming an essential mopi, has the value one. These may be eliminated because they will never appear in a minimal expression. Similarly step 2)-c)-ii) is used to eliminate mopi which imply equally simple mopi if all possible minimal expressions are not required. Finally, step 2)-d) is used to eliminate columns which imply other columns and thereby reduce the size of the prime implicant table.

This procedure will now be applied to a very simple example.

Example 2: We are given two incomplete single-output truth functions and we wish to find the simplest equivalent multiple-output expression. The functions are

$$F_1 = G_1 = X_1X_2X_3' + X_1'X_2'X_3' + Z_{1,3}X_1'X_2X_3 + Z_{1,2}X_1'X_2X_3'.$$

$$F_2 = G_2 = X_1X_2'X_3' + X_1'X_2X_3' + Z_{2,1}X_1'X_2'X_3 + Z_{2,0}X_1'X_2'X_3'.$$

We assign $Z_{1,3} = Z_{1,2} = Z_{2,1} = Z_{2,0} = 1$ and find G_3 which is:

$$G_3 = X_1'X_2X_3' + X_1'X_2'X_3'.$$

The prime implicants are listed in Table VII. Using this list and the required minterms $f_{1,0}$, $f_{1,6}$, $f_{2,4}$ and $f_{2,2}$, we can construct Prime Implicant Table VIII. Upon inspecting the rows we see there are no check marks in the rows corresponding to $y_1X_1'X_2$ and $y_2X_1'X_2'$, so these rows are deleted. We observe only one check mark in the columns corresponding to the required minterms $y_1X_1X_2X_3'$ and $y_2X_1X_2'X_3'$, so $y_1X_2X_3'$ and $y_2X_2'X_3'$ are essential mopi. These rows and columns are deleted

[14] S. R. Petrick, "A Direct Determination of the Irredundant Forms of a Boolean Function From the Set of Prime Implicants," AF Cambridge Res. Center, Bedford, Mass., Tech. Rept. 110; April, 1956.

TABLE VII
LIST OF PRIME IMPLICANTS FOR EXAMPLE 2

Prime Implicants	Corresponding mopi
$F_1: x_2 x_3'$	$y_1 x_2 x_3'$
$x_1' x_3'$	$y_1 x_1' x_3'$
$x_1' x_2$	$y_1 x_1' x_2$
$F_2: x_2' x_3'$	$y_2 x_2' x_3'$
$x_1' x_3'$	$y_2 x_1' x_3'$
$x_1' x_2'$	$y_2 x_1' x_2'$
$G_3: x_1' x_3'$	$(y_1 + y_2) x_1' x_3'$

TABLE VIII
TABLE OF PRIME IMPLICANTS FOR EXAMPLE 2

MOPI \ MOM	$y_1\ x_1\ x_2\ x_3'$	$y_1\ x_1'\ x_2'\ x_3'$	$y_2\ x_1\ x_2'\ x_3'$	$y_2\ x_1'\ x_2\ x_3'$
$-y_1 - x_2 - x_3'-$	✓			
$y_1\ x_1'\ x_3'$		✓		
$=y_1 : x_1' : x_2=$				
$-y_2 . x_2' . x_3'-$			✓	
$y_2\ x_1'\ x_3'$				✓
$=y_2 : x_1' : x_2'=$				
$(y_1 + y_2)\ x_1'\ x_3'$		✓		✓

Essential Terms: $y_1x_2x_3'$ and $y_2x_2'x_3'$.

and a Revised Prime Implicant Table IX is constructed. From this it can be seen that

$$G = (y_1 + y_2)X_1'X_3' + y_1X_2X_3' + y_2X_2'X_3'$$

can be constructed using both a minimum number of diodes and gates.

The multiple-output prime implicant defined in this paper is a generalization of the single-output prime implicant *for completely specified multiple-output functions.* Incompletely specified truth functions are accommodated by the generalization of an artifice previously described by Phister. Because of the manner in which "don't cares" are handled in this particular procedure when dealing with an incompletely specified truth function, many of the terms found in step 1)-c) are not useful and will be eliminated during subsequent steps. Although for convenience these terms will still be referred to as mopi, the reader is reminded that a complete general multiple-output prime implicant has not been defined here, nor is such a concept necessary. McNaughton and Mitchell[15] have, however, previously described the *rth-order prime implicant* which is an extension of the prime implicant concept for incompletely specified multiple-output networks in which the unspecified cases ("don't cares") are the same for all outputs. In addition, they describe a procedure for identifying these rth order prime implicants and make use of them in a minimization procedure. While the algorithm described here differs significantly from their procedure the essential terms and the mopi remaining after step 2)-c) do correspond to their rth-order prime implicants. They also discuss what they consider to be an appropriate definition of prime implicant when the unspecified cases for the various outputs are not necessarily the same but do not describe a procedure for identifying such prime implicants or make further use of them. The essential terms and the mopi remaining after step 2)-c also satisfy this definition.

TABLE IX
REVISED TABLE OF PRIME IMPLICANTS FOR EXAMPLE 2

MOPI \ MOM	$y_1\ x_1'\ x_2'\ x_3'$	$y_2\ x_1'\ x_2\ x_3'$	WEIGHT (DIODES REQUIRED)
$y_1\ x_1'\ x_3'$	✓		3
$y_2\ x_1'\ x_3'$		✓	3
✓ $(y_1 + y_2)\ x_1'\ x_3'$	⊘	⊘	4

The check marks designate the nonessential mopi selected.
The circles denote the multiple-output minterms which subsume this mopi.

The generalized Quine rules as stated here can be used to simplify both single- and multiple-output Boolean expressions with and without redundancies since, as previously stated, for the purpose of this discussion, single-output expressions are considered to be special cases of multiple-output expressions. It is believed that these modified Quine rules may serve as a basis for a computer program and that some existing programs based on the Quine rules may easily be modified to apply to the simplification of multiple-output networks.

[15] R. McNaughton and B. Mitchell, "The minimality of rectifier nets with multiple outputs incompletely specified," *J. Franklin Inst.*, vol. 264, pp. 457–480; December, 1957.

Uniqueness of Weighted Code Representations*

G. P. WEEG†, MEMBER, IRE

Summary—Decimal computers ordinarily use a binary-coded decimal representation. One class of binary-coded decimal digits is the so-called four-bit weighted code representation with weights w_1 w_2 w_3 w_4. Each w_i is a nonzero integer in the range $-9 \leq w_i \leq 9$, and the set of weights must have the property that every decimal digit can be represented by the sum

$$\sum_{i=1}^{4} b_i w_i,$$

with the b_i being 0 or 1.

For some weighted codes the weights are such that some digits can be represented by more than one sum of the specified form. For example, the 7421 weighted code has the property that 7 may be represented either as 1000 or as 0111.

This paper produces a necessary and sufficient condition on the weights of a weighted code for the unique representation of each digit by a sum of the specified form. Further, all possible sets of weights are displayed.

Introduction

BINARY-coded decimal digits are used in many decimal computers, with some using so-called weighted codes. Both Caldwell[1] and Richards[2] discuss weighted codes, with the latter producing a table including seventeen four-bit weighted codes with positive weights. Richards does not state that these constitute all possible positive weighted four-bit codes, but that such is the case is proved in the present paper.

A four-bit weighted code with weights w_1 w_2 w_3 w_4 where w_i is a nonzero integer in the range $-9 \leq w_i \leq 9$ (for $i = 1, 2, 3, 4$) is a set of ten four-bit numbers of the form b_1 b_2 b_3 b_4, such that if n is any integer in the range $0 \leq n \leq 9$, then

$$n = \sum_{i=1}^{4} b_i w_i \qquad (1)$$

for some combination of the b_i, with each b_i either 0 or 1. By definition each four-bit weighted code represents each of the integers from 0 through 9 uniquely.

It is the case, however, for certain sets of weights, that some integers n (where here and hereafter n is in the range $0 \leq n \leq 9$) can be represented by more than one four-bit number. Thus, for example, using the set of weights 8421, there is but one representation of each integer n as a four-bit number. But if one uses the set of weights 3321, one sees that the integer 3 can be represented 1000, 0100, or 0011.

This paper is concerned primarily with determining which sets of weights can be used to represent all the integers n uniquely in the form (1).

The Range of the Weights

Some results concerning the size and sign of the weights are easily obtained.

Lemma 1: In a four-bit weighted code with all positive weights w_1 w_2 w_3 w_4, at most one weight can exceed 4.

Proof: If more than one weight exceeds 4, then at most two weights, say w_{i_1} and w_{i_2}, where these are some two of the weights w_1 w_2 w_3 w_4, are less than or equal to 4. But then the digits 1, 2, 3 and 4 must be represented by linear combinations of w_{i_1} and w_{i_2} with coefficients 0 or 1. But at most, three nonzero combinations of w_{i_1} and w_{i_2} exist. Hence, no more than one weight can exceed 4.

Lemma 2: At most two weights in a four-digit weighted code with weights w_1 w_2 w_3 w_4 can be negative.

Proof: If more than two weights are negative, then suppose that w_{i_1}, w_{i_2}, and w_{i_3} are negative. Hence, the number of non-negative combinations of the four weights is at most 9. But ten non-negative integers must be represented, which is impossible with only at most 9 combinations available. Hence, at most, two weights can be negative.

Lemma 3: The only four-digit weighted codes with all positive weights are those listed by Richards.[3]

Proof: The proof[4] is straightforward and will only be described here. Every positive weighted code must have 1 as one weight. A second weight must be 1 or 2. A third weight must be 1, 2, 3, or 4. Finally the last weight must be one of 2, 3, $\cdots$, 9. The sum of all the four weights must be at least 9. Hence, one can produce the diagram of Fig. 1.

Those codes in the display of Fig. 1, checked to indicate that they are weighted codes, are:

1125*	1224*	1236*	1246*
1134*	1225*	1237*	1247*
1135*	1226*	1242	1248*
1136*	1233*	1243	
1143	1234*	1244*	
1215	1235*	1245*	

Eliminating duplications leaves exactly the seventeen four-digit codes Richards listed,[5] which are marked here by asterisks.

* Received by the PGEC, March 5, 1960; revised manuscript received, July 15, 1960.

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[1] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y.; 1958.

[2] R. K. Richards, "Arithmetic Operations in Digital Computers," D. Van Nostrand Co., Inc., New York, N. Y.; 1955.

[3] *Ibid.*, p. 178.

[4] The author is indebted to R. R. Brown and B. H. Barnes for this lemma and its proof.

[5] Richards, *op. cit.*, p. 178.

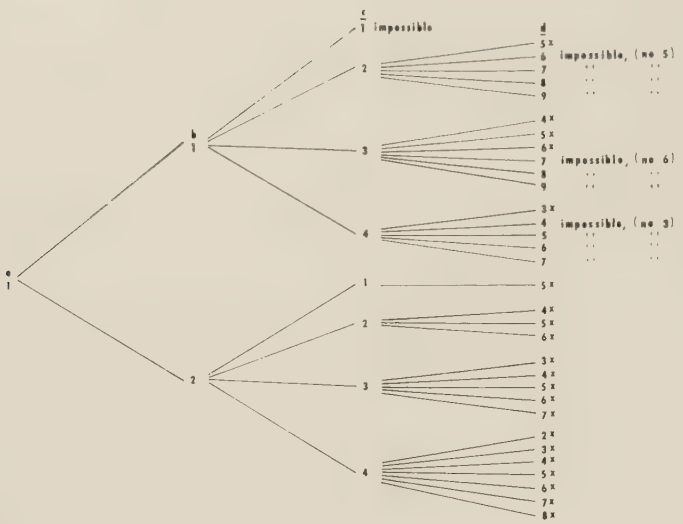

Fig. 1.

Uniqueness of Representation

Lemma 4: The only four-bit weighted code with all positive weights which represents the digits 0 through 9 uniquely is the 8421 code.

Proof: Any positive weighted code must have 1 for one weight. The second weight is 1 or 2, and to be unique, must be 2. The third digit can then be 1, 2, 3, or 4, but for uniqueness, the third digit must be 4. Finally, the fourth digit can be 2 through 8. However, 2 through 7 can be represented by combinations of 1, 2, 4. Hence, the only four-digit weighted code with positive weights which represents each digit 0 through 9 uniquely is 8, 4, 2, 1.

In a four-bit weighted code with weights $w_1\ w_2\ w_3\ w_4$, which are not necessarily all positive, if some integer n has two representations, say

$$n = \sum_{i=1}^{4} b_i\, w_i = \sum_{i=1}^{4} \bar{b}_i\, w_i, \tag{2}$$

where b_i and $\bar{b}_i$ are 0 or 1, for $i=1, 2, 3, 4$, then there exists a set of coefficients $\beta_1, \beta_2, \beta_3, \beta_4$, where each β_i is 0, 1, or -1, such that

$$\sum_{i=1}^{4} \beta_i\, w_i = 0. \tag{3}$$

In fact, $\beta_i = b_i - \bar{b}_i$, and since b_i and $\bar{b}_i$ are each 0 or 1, then β_i is 0, 1, or -1.

The following question then suggests itself: Can (3) be true for a set of weights $w_1\ w_2\ w_3\ w_4$, and, at the same time, can each integer n be represented uniquely by a sum of the form (1)? For example, might it be possible that two representations (using the set of weights $w_1\ w_2\ w_3\ w_4$) of an integer greater than 9 exist, causing (3) to be true, while at the same time each integer 0 through 9 is uniquely represented by sums of the form (1)? The answer is that if (3) is true for a set of weights $w_1\ w_2\ w_3\ w_4$, then some integer n can be represented in more than one way by a sum of the form (1).

Theorem 1: All the integers n in the range $0 \leq n \leq 9$ are represented uniquely by sums of the form (1) if and only if

$$\sum_{i=1}^{4} \beta_i \omega_i \neq 0$$

for any set of coefficients $\beta_1, \beta_2, \beta_3, \beta_4$ chosen from the s 0, 1, -1, except for all $\beta_i = 0$.

Proof: Suppose some integer n is not represente uniquely by a sum of the form (1). Then for that there are coefficients b_i and $\bar{b}_i$ $(i=1, 2, 3, 4)$, such th (2) and hence (3) are true. Hence, if

$$\sum_{i=1}^{4} \beta_i w_i \neq 0,$$

except for all $\beta_i = 0$, it follows that each integer n represented uniquely by a sum of the form (1).

On the other hand, suppose each integer n is repr sented uniquely by a sum of the form (1). If the set weights $w_1\ w_2\ w_3\ w_4$ is such that all w_i are positive, the the set is 8421 by Lemma 4 (or some permutation it). But as can be verified, no sum of the form

$$8\beta_1 + 4\beta_2 + 2\beta_3 + \beta_4 \tag{4}$$

vanishes, for the β_i chosen from the set 0, 1, -1, oth than for all $\beta_i = 0$.

If some of the weights in the set $w_1\ w_2\ w_3\ w_4$ are neg tive, we will show that if each integer is represente uniquely by a sum of the form (1), then

$$\sum_{i=1}^{4} \beta_i\, w_i \neq 0$$

except for all $\beta_i = 0$. To do so we will consider the valu of the coefficients $\beta_1, \beta_2, \beta_3, \beta_4$, assuming that

$$\sum_{i=1}^{4} \beta_i\, w_i = 0$$

for some set of β_i not all of which are zero.

a) Suppose that all of the β_i are non-negative. The the integer 0 has two representations, namely as

$$\sum_{i=1}^{4} 0 \cdot w_i \quad \text{and as} \quad \sum_{i=1}^{4} \beta_i \cdot w_i,$$

contrary to hypothesis.

b) Suppose that exactly one coefficient is negative. is not an essential restriction to suppose that $\beta_1 = -$ Then,

$$w_1 = \beta_2\, w_2 + \beta_3\, w_3 + \beta_4\, w_4. \tag{5}$$

If $w_1 > 0$, then the integer w_1 has two representation contrary to hypothesis. If $w_1 < 0$, then by Lemma 2, e actly one of the weights w_2, w_3, w_4, must be negativ Again, suppose that $w_2 < 0$. Then if neither β_3 nor β_4 a zero, we have

$$w_1 = w_2 + w_3 + w_4, \tag{6}$$

so that the sum of w_2 and any other weight w_i is neg tive. Hence, the only possible positive combinations w_1, w_2, w_3, and w_4 are those of w_1, w_3, and w_4. But the fewer than six combinations of w_1, w_2, w_3, and w_4 a

sitive. Hence, if exactly one coefficient is negative d none of the other coefficients vanish, then $w_1\ w_2\ w_3$ are not the weights of a four-bit weighted code.

Suppose next, then, that w_1 and w_2 are still negative d one of β_3 and β_4 is zero, say $\beta_4=0$. Then,

$$w_1 = w_2 + w_3, \tag{7}$$

d w_1, w_2, w_1+w_2, w_2+w_3, and $w_1+w_2+w_3$ are all nega-re. This leaves only eleven possible non-negative com-nations of the w_i. But from (7)

$$w_1 + w_4 = w_2 + w_3 + w_4, \tag{8}$$

that, at most, ten of these combinations are distinct. nally, $w_1+w_4\leq 9$, since $w_1<0$ and $w_4\leq 9$. Hence, if $\leq w_1+w_4\leq 9$, then there is a nonunique representa-on for the integer w_1+w_4, that given by (8). If w_1+w_4 0, then there are only, at most, nine non-negative mbinations of the w_i, while ten such combinations are eded for the set w_1, w_2, w_3, w_4 to be the weights of a eighted code. Thus, if $\beta_1<0$ and $\beta_4=0$, while $\beta_2=\beta_3=1$, en either $w_1\ w_2\ w_3\ w_4$ are the weights of a nonunique ur-bit weighted code, or else $w_1\ w_2\ w_3\ w_4$ are not the eights of a four-bit weighted code.

For the last part of this argument, suppose that w_1 d w_2 are still negative, while $\beta_3=\beta_4=0$. Then,

$$w_1 = w_2. \tag{9}$$

nce $w_1+w_3=w_2+w_3$ and $w_1+w_4=w_2+w_4$, then if any these four sums are not negative there is some integer represented by two sums of the form (1). Hence, w_1, , w_1+w_2, w_1+w_3, w_2+w_3, w_1+w_4 and w_2+w_4, are all gative, so that there are not ten non-negative com-nations of the form (1). Therefore, if $\beta_3=\beta_4=0$, $w_2\ w_3\ w_4$ are not the weights of a four-bit weighted de.

We can conclude then, that if precisely one coefficient is negative and

$$\sum_{i=1}^{4} \beta_i\, w_i = 0,$$

at either $w_1\ w_2\ w_3\ w_4$ are not the weights of a four-bit eighted code, or else the hypothesis of uniqueness is olated.

c) Next, suppose that exactly two coefficients, say and β_2 are negative. Then,

$$w_1 + w_2 = \beta_3\, w_3 + \beta_4\, w_4. \tag{10}$$

$w_1+w_2>9$, then all four weights are positive, and this se has already been disposed of. If $0\leq w_1+w_2\leq 9$, then ere is a nonunique representation for the integer $+w_2$, contrary to hypothesis. If $w_1+w_2<0$, w_1+w_2 $\beta_3w_3+\beta_4w_4$. Suppose that w_1 and w_3 are negative. nen $\beta_3=1$, so that

$$w_1 + w_2 = w_3 + \beta_4\, w_4. \tag{11}$$

If $\beta_4=1$, then $w_1+w_2=w_3+w_4$, so that w_1, w_3, w_1+w_2, $+w_3$, $w_1+w_2+w_3$, w_3+w_4, and $w_1+w_3+w_4$ are all gative. But this leaves only nine non-negative com-nations of the form (1) whereas ten are required. ence $w_1\ w_2\ w_3\ w_4$ in this case are not the weights of a four-bit weighted code. If $\beta_4=0$, then $w_1+w_2=w_3$. Since then $w_1+w_2+w_4=w_3+w_4$, it must be the case that $w_3+w_4<0$ (for otherwise there is a nonunique representation for the integer w_3+w_4). Hence, w_1, w_1+w_2, w_3, $w_1+w_2+w_3$, w_3+w_4, $w_1+w_2+w_4$ and w_1+w_3, are all negative so that $w_1\ w_2\ w_3\ w_4$ are not the weights of a four-bit weighted code.

Thus, if exactly two coefficients among the β_i are negative, then either $w_1\ w_2\ w_3\ w_4$ are not the weights of a four-bit weighted code, or else the uniqueness hypothesis is violated.

d) If three or four of the β_i are negative, the argument is similar to that in parts a) and b). This completes the proof of Theorem 1.

Using this theorem, we shall proceed to determine the four-bit weighted codes which have the property that each digit n is represented uniquely by sums of the form (1). We first determine the set of all four-bit weighted codes in the next section.

A Complete List of all Four-Bit Weighted Codes

Since by Lemma 2 a weighted code can have at most two negative weights, one can determine all of the weighted codes by examining all $9\cdot 9\cdot 18\cdot 18=4\cdot 9^4$ combinations $w_1\ w_2\ w_3\ w_4$, where $0<w_i\leq 9$, $i=1$, 2 and $-9\leq w_j\leq 9$ for $j=3$, 4 with $w_j\neq 0$. However, the number of such combinations can be reduced by $2\cdot 9^4$ by observing that there are $9\cdot 9\cdot 9\cdot 9$ combinations with the first three weights positive and the last weight negative, and that there are $9\cdot 9\cdot 9\cdot 9$ combinations with the first two weights positive and the last two negative. Hence, a total of $2\cdot 9^4$ combinations of weights $w_1\ w_2\ w_3\ w_4$ need to be examined in order to determine all weighted codes with one or two negative weights.

A program for the MISTIC computer was written by John Barth to determine these weighted codes. The program was designed to generate all $2\cdot 9^4$ combinations of $w_1\ w_2\ w_3\ w_4$ with the first two weights positive and the last two negative, and with the first three weights positive and the last one negative. Then all sixteen combinations of $w_1\ w_2\ w_3\ w_4$, in each case, were formed. If the digits 0 through 9 were then included in the sixteen combinations, that set of weights was output as the weights of a weighted code.

The following list is the set of all four-bit weighted codes so obtained with one or two negative weights. Those with all positive weights are found in Lemma 3. Those followed by the symbol & are such as to represent each integer n uniquely by a sum of the form (1):

861-4&	852-4&	843-6&	843-2&	842-5&
842-3&	842-1&	841-6&	841-2&	832-4&
821-4&	763-5&	753-6&	751-4	751-3
742-1	741-2	732-1	731-2	721-4
721-3	654-3	653-7&	653-4	652-4
651-3	643-5	643-2	642-3	642-1
641-2	632-4	632-2	632-1	631-2
631-1	622-1	621-4	621-3	621-2
543-6	543-3	543-2	542-3	542-1
541-2	532-1	531-2	531-1	522-1
443-2	442-1	441-2	432-1	—
18-2-4&	27-1-3	27-1-4	28-1-4&	36-1-1
36-1-2	37-1-2	38-2-4&	45-1-2	46-1-2
47-1-2	48-1-2	48-2-3&	57-1-3	58-2-4&
68-1-4&	78-2-4&.			

Analog Representation of Poisson's Equation in Two Dimensions*

R. J. MARTIN†, N. A. MASNARI†, AND J. E. ROWE†

Summary—A new analog device, called a Poisson cell, has been developed which aids in obtaining solutions to either Laplace's equation or Poisson's equation. The cell may be used to simulate such potentials as electric potential, magnetic potential, gravitational potential, and the velocity potential of irrotational flow; it has applications in the fields of hydrodynamics, heat conduction, and aerodynamics.

The cell is a solid volume-conducting medium made from a homogeneous mixture of hydrostone and graphite. Electrode configurations may be painted on the surface with conducting paint or imbedded directly in the structure. In the case of Poisson's equation, where $\nabla^2\phi(x, y)=f(x, y)$, the function $f(x, y)$ is simulated by injecting currents into the underside of the cell.

The application of the Poisson cell to numerous problems and in particular to problems in electron flow is discussed in detail, along with the incorporation of the cell into either an analog computer system or a combined analog-digital computer system.

Introduction

IN THE FIELDS of mathematics, engineering and physics, a great many physical problems arise involving the solution of both Laplace's equation and Poisson's equation in two independent variables. Poisson's equation, in particular, is involved in the study of space-charge control tubes and in the design of electron injection systems for microwave electron devices.

In general these problems can be solved by formal methods only for a restricted class of regular geometries and types of boundary conditions. Analog techniques, such as the electrolytic tank, the resistance board and the rubber membrane, have been developed to handle the more complicated problems. Also the use of complex numerical methods on high-speed digital computers has permitted the solution of previously insoluble problems involving Laplace's equation. When problems involving Poisson's equation are encountered, however, these analog methods are inadequate and the analytical and digital methods become extremely cumbersome. The digital computer methods usually offer high accuracy but a great deal of computation time is needed when a problem involving a wide variety of boundary conditions is encountered. Several important references to the above other methods used in solving the Laplace and Poisson equations are given below.[1–6]

An analog device, called a Poisson cell,[7] has been d veloped which permits the solution of Poisson's equ tion where the density of sources and sinks varies in t dimensions in either rectangular or cylindrical coor nates. The Poisson cell is a solid volume-conducti medium which may be used in conjunction with an a alog computer or an analog-digital combination. T geometrical boundaries are established in the cell either imbedding electrodes in the cell or painting th on the surface with conducting paint. The desired fi pattern is then set up by applying the proper potenti to the electrodes. The cell is essentially a two-dime sional nonlinear function generator in which the volta of the analog becomes the analog of the potential, of Poisson's equation. The volume-conducting mater is shaped in the proper form for simulating eit rectangular, polar or cylindrical geometries. In t application of the cell the potential of Poisson's equ tion is separated into two parts such that one co ponent is due to the boundary potentials and the oth component is due to the distribution of sources or sin in the cell.

In order to simulate a distribution of sources a sinks for Poisson's equation, a matrix of dots is appli to the underside of the cell, and current is inject through these sources so that regions of uniform cu rent density are produced in the cell which simula regions of uniform source or sink distribution in t actual device being simulated. In this manner a co tinuous density distribution is represented in the Poi son cell by a discontinuous staircase density distrib tion of currents. Potentials or gradients are then mea ured by moving probes over the surface of the ce DC potentials are used throughout the system, th making it particularly advantageous for use with analog computer.

The Poisson cell is used to solve boundary value a initial condition problems in compressible lamin fluid flow. The cell allows variation of the density

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urces in two dimensions in any geometry. It can be st advantageously applied to design problems where e is interested in determining boundary conditions obtain a desired condition of fluid flow. For such a oblem, the engineer can quickly obtain an intuitive l for the manner in which the fluid flow is affected the changing of various boundaries and initial con-tions.

Applications of the Poisson Cell

In the past, most field simulating work has been car-d out using an electrolytic tank or a rubber-mem-ane analog. The membrane method is very limited d the tank has several disadvantages, one being the cessity of using ac voltages to avoid polarization effects. he use of ac introduces errors due to stray voltage ckup. The variation of electrolyte conductivity with me and the meniscus effect of water are other serious roblems in the tank. These obstacles do not exist with solid volume-conducting medium.

The Poisson cell is a homogeneous mixture of hydro-tone and graphite in which the hydrostone serves as a natrix with the graphite particles forming volume-onducting paths throughout the structure. The re-stivity is determined by the amount of graphite, while ne linearity is inversely proportional to the resistivity. or plates with resistivities in the vicinity of 10 kΩ er square, uniformities of better than one per cent can asily be obtained.

As pointed out in the previous section, the plates an be made in any shape including rectangular (x, y), edge (r, z) and polar (r, θ) geometries. The wedge is sed to simulate an angular section of a cylindrical eometry in which the source free dc potential distribu-on must be logarithmic with radius. The cell can be sed to simulate either Laplace's $\nabla^2\phi(x, y) = 0$ or Pois-on's equation $\nabla^2\phi(x, y) = f(x, y)$, where ϕ could be any ne of several types of potentials and $f(x, y)$ is a density unction. The potentials which can be simulated in-ude 1) electric potential, 2) magnetic potential, 3) ravitational potential, 4) velocity potential of irrota-onal motion of an incompressible fluid as used in hy-rodynamics and aerodynamics, and 5) temperature in homogeneous solid.

The most interesting problem is encountered when the gions being studied contain sources. This requires the olution of Poisson's equation where $f(x, y)$ is the ensity of sources. In the case of the electric potential $x, y)$ becomes $\rho(x, y)$, which is the space-charge density nd can be either positive or negative. The quantity $x, y)$ creates a distortion in the field produced by the eometrical boundary potentials and is simulated in the ell by injecting currents into dots painted on the under-de of the plate. Each dot is connected through a 1-egohm resistor to a power supply and current is either jected (source) or withdrawn (sink) through the dot; us the field on the top of the cell is correspondingly storted. At all points where sources exist, Poisson's equation must be satisfied; while in regions free of these sources, Laplace's equation still holds.

In the above applications the cell was used to study potential problems of a very general type. It can also be used as a nonlinear function generator by simply painting the desired function on the surface of the cell with conducting paint. The function may also be distorted or changed in a prescribed manner by injecting current into the underside of the cell. The magnitude of current injected may be related to a third variable of the system.

Application to Electron Flow Problems

In this laboratory the Poisson cell has been applied to the determination of electron beam trajectories in both crossed electric and magnetic fields and in axially symmetric systems where the magnetic field is along the direction of primary electron flow. These, of course, are problems involving the solution of Poisson's equation. These trajectories are at present being studied with the conditions of steady-state electrode potentials and uniform magnetic fields. The assumptions that must apply are: no crossing of trajectory paths and no collisions between electrons. The results desired are the electron stream trajectories and the magnitudes of space-charge-limited current flow for a given electrode configuration.

The complete setup required to determine electron trajectories consists of a Poisson cell, an analog computer, two X-Y plotters and a current source panel. The flow diagram is shown in Fig. 1.

The Poisson cell is constructed to simulate the particular tube geometry to be studied. The currents injected into the cell to simulate space charge are fed from the connections to the current sources panel as shown in Fig. 2. The Poisson cell is placed upon the plotting surface of a converted X-Y plotter. The pen

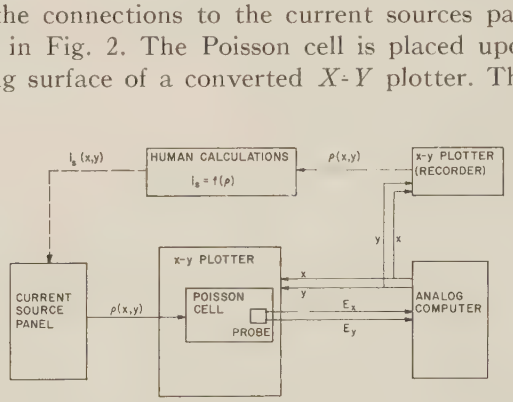


Fig. 1—Flow diagram illustrating interconnections between various components.

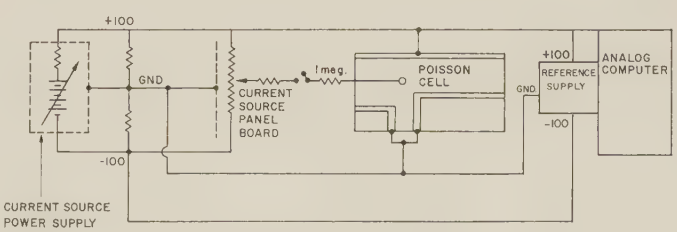


Fig. 2—Circuit used to inject current into the Poisson cell to simulate space charge.

carriage of this plotter has been replaced by a probe mechanism that is moved over the Poisson cell surface by varying the X and Y input voltages to the plotter.

The probe mechanism shown in Fig. 3 consists of a five-point probe assembly that will permit the measurement of potential and potential gradient that is to be continuously taken from the Poisson cell. As seen in Fig. 4, V_5 measures the Poisson cell potential. For the five-probe system, the gradients are determined approximately in the following manner.

$$-\frac{dV}{dx} = \frac{V_3 - V_1}{2l} \tag{1}$$

and

$$-\frac{dV}{dy} = \frac{V_4 - V_2}{2l}. \tag{2}$$

The space-charge density, as a function of x and y, can also be approximately determined in the following manner.

$$\nabla^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2}$$

$$= -\frac{\rho}{\epsilon} \approx \frac{1}{l^2}(V_1 + V_2 + V_3 + V_4 - 4V_5). \tag{3}$$

Thus the space charge being simulated at any point can be determined by the knowledge of the five potentials. When there is no space charge a four-point probe system may be used. The potential and potential gradients read from the Poisson cell are then fed to the analog computer by means of unloading amplifiers. This was necessitated because the small areas of contact of each probe upon the surface of the Poisson cell produce a high contact resistance. The unloading amplifier allows the proper voltage to be fed into the computer while bypassing all noise signals.

An analog computer is used to solve the ballistic equations for determining the electron trajectories. Fig. 5 shows the computer diagram of the problem for the four-probe system. The second X-Y plotter is used to record the trajectories of the electron stream. From these plots the space-charge distribution of the particular tube geometry is determined. This distribution is then set into the Poisson cell by adjustments of the current sources. The human element is used here because it was determined that automatic means would be too expensive to install initially. However, several automatic methods are possible and one of them is discussed later. The current injection system, plotter and the Poisson cell are all shown in Fig. 6.

The Poisson cell and computer together form a closed loop system; *i.e.*, gradients measured by the probes on the cell are continuously fed to the computer, where the electron ballistic equations are solved and the probe position is determined. In this manner the probe moves over the cell as an analog of a specific electron in the actual tube and measures the field that such an electro would find there.

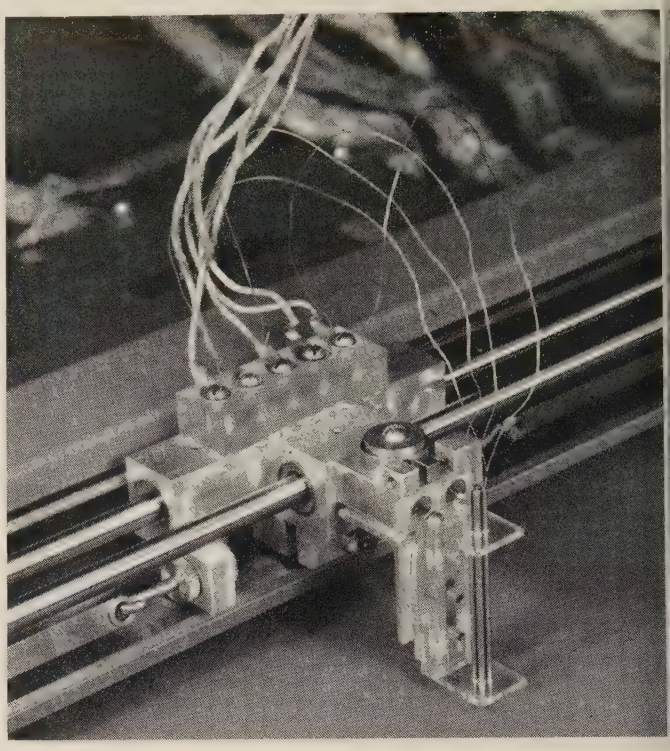


Fig. 3—Probe-carriage assembly.

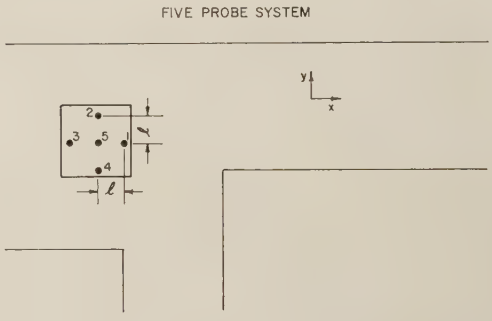
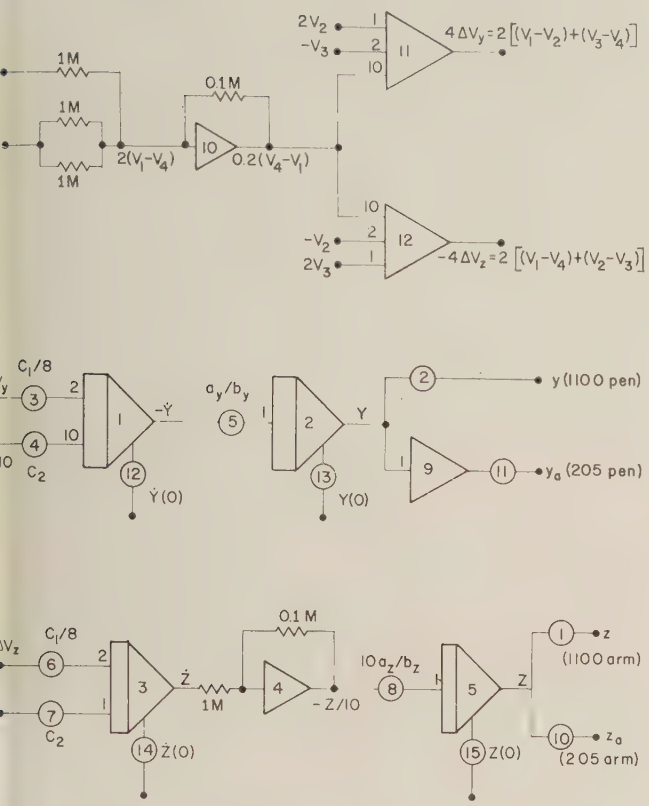


Fig. 4—Five-probe method of measuring potential and potential gradients.

To solve a specific electron beam problem with onl boundary and initial conditions given, a self-consister method is utilized that rapidly converges to the desire solution. The electron trajectories are first found for space-charge-free case; then the space-charge distribu tion is determined from the complete series of traje tories. This distribution is set into the Poisson cell an the trajectories are repeated. Such a procedure is co tinued until the space-charge distribution converges a consistent distribution, *i.e.*, two repeated determin tions of $\rho(x, y)$ are identical.

Space charge is simulated in the Poisson cell in di crete segments by injecting currents in proportion the space-charge density and area elements. Each cu rent is supplied from the current source panel throug separate high-impedance circuits. With such hig impedance sources, the loading effect of one upon a other is generally negligible.



g. 5—Diagram illustrating the solution of the ballistic equations, which are: $b_yP^2y=C_1\Delta V_y-C_2Z$ and $b_zP^2z=C_1\Delta V_z+C_2Y$. (Four probe system.)

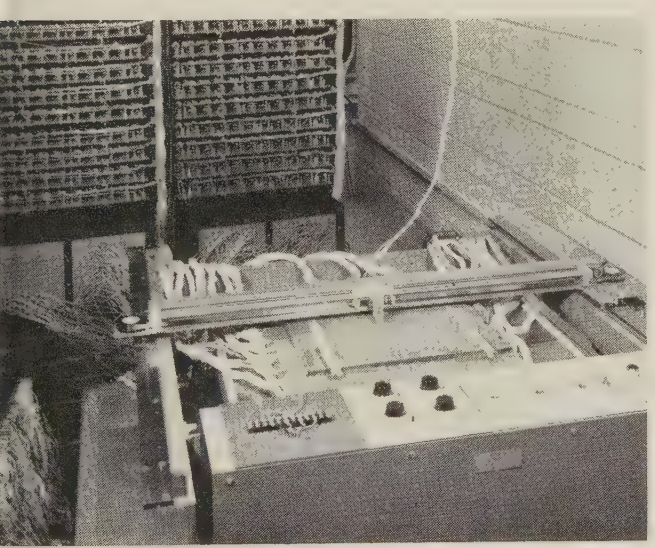


Fig. 6—Poisson cell, plotter and current injection system.

The accuracy of the Poisson cell is basically deter-ined by the size of the area elements of the space-harge representation. A continuous space-charge dis-ibution in the actual tube is represented by a discon-nuous staircase distribution in the Poisson cell. Thus egions in which the space-charge is abruptly changing equire smaller area elements in the analog to obtain a ven accuracy of representation. The proper design onsideration is to use area elements in the Poisson cell such a size as to give errors in the space-charge dis-tribution of the same order as the uniformity of resistivity of the cell, which is approximately two per cent. In general, the size of the cell and the smallness of the space-charge area elements are limited by the number of current sources available. In our installation, each of the available 1584 current sources represents an area of approximately 10^{-4} square inches in the actual tube.

Another error which arises is that in the probe pick-up system. Though gradients of the potential are desired, the probe system gives differentials of the potential. This error is larger in regions where space charge is large.

In the process of obtaining trajectories, the errors derived during the initial part of the run are the most important since they accumulate as the run proceeds. The two major sources of error are due to the probe pick-up mechanism. First, as mentioned above, the probe is reading the differential of the potential and not the true gradient. This error can accumulate throughout the run. It must be noted that this error is a function of position of the probe and thus cannot be reduced by time scaling. It may be reduced only by decreasing the size of the probe. The second source of error is sticking of the probes. This effect can be minimized by proper design of the probe holder. During a run, these probes tend to bounce and friction in the probe holder tends to prevent them from immediately returning to the plate and making contact with it. The best way to minimize this second error is to keep the probe carriage and probes as clean as possible and to adjust the X-Y plotter servos so that the probe carriage "jitters" slightly. In general, if the probe carriage is sticking, it can be easily determined during a run by observing the error circuit output in the computer. The error checking circuit continuously compares the kinetic energy of the particle with its potential energy along the trajectory. This error circuit is illustrated in Fig. 7.

The use of unloading amplifiers between the probe pick-ups and the computer does not appear to give appreciable error as long as trajectories are run slowly enough to be unaffected by the time constant of the unloading amplifiers. The accuracy of adjustment of the unloading amplifiers to obtain the unloading condition is quite critical. Noise in the pick-up system is bypassed and is negligible. The computer time for each trajectory is approximately 30 seconds and thus drift error in the computer is negligible. Generally, the error indicated by the energy balance equation after a trajectory is of the order of three per cent. Repeatability of an electron trajectory is good and the cumulative error in the error circuit is also reproducible. This indicates that the major error is caused by the method of measuring gradients.

Aside from simulating static magnetic and electric fields, the Poisson cell can be applied to study most problems involving electron flow. It can be used in studies of electron beam or electron microscope focusing if the requirement of laminar flow is approximately

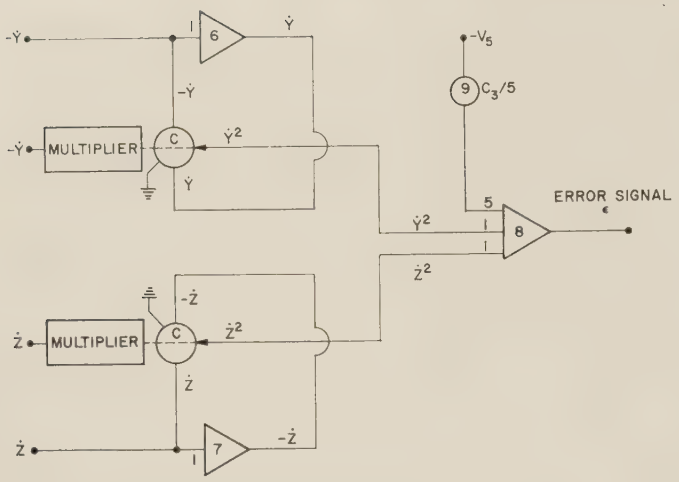


Fig. 7—Error circuit where ϵ is the error in the energy equation $-\dot{Y}^2-\dot{Z}^2+C_3V_5=\epsilon$.

met. In such cases, two Poisson cells or more would be operated in parallel. One of the cells would be made to represent the electric field of the problem in question, while the other cells would give a representation of the magnetic flux vector. A separate cell would be necessary to represent each component of the flux vector [*i.e.*, $B_x(x, y, \cdots), B_y(x, y, \cdots), \cdots$]. All of these separate components would then be fed into an analog computer, where the ballistic equations would be solved.

Another interesting field of study would be that of transit time effects upon an electron beam. Time-varying potentials would be applied to the electrodes to simulate ac electric fields. However, because it would be difficult to obtain a time-changing space-charge distribution, such an application would necessarily be limited to the small-signal case (*i.e.*, $\rho_{d-c} \gg \rho_{a-c}$).

Analog-Digital Automatic System

It was mentioned in previous sections that sources are represented by the injection of currents into the dots on the bottom of the cell. Regardless of the type of potential being considered, problems concerned with Poisson's equation are all similarly solved. Thus the method discussed below for a special case can be easily adapted to any of the other possible problems.

Laminar electron flow in a tube will be investigated and the method of solving Poisson's equation illustrated. In the discussion to follow, the subscript t will indicate actual tube parameters, while the s subscript will indicate the cell parameters.

It can be shown that the current injected (i_s) into a cell volume element ($d\tau_s$) is related to the space-charge density (ρ_t) in the actual tube by:

$$i_s = \kappa \rho_t d\tau_s, \tag{4}$$

where κ is a constant for a particular cell.

Furthermore, under the assumption of laminar flo ρ_t can be written as

$$\rho_t = \frac{MGJ_c}{\sqrt{V_s}},$$

where

M = constant of the cell,
J_c = current density at cathode of the actual tube,
V_s = potential at point in question in the cell, and

$$G = \frac{\text{beam width at cathode}}{\text{beam width at point in question}}.$$

Thus (4) becomes:

$$i_s = \frac{NGJ_c d\tau}{\sqrt{V_s}}$$

where N = constant.

For any given tube, only a knowledge of J_c, $d\tau$, an G at a point is required to determine the proper curre to be injected into the source associated with the poin In general, the J_c value being used can be easily dete mined by measurements of total cathode current an cathode area.

As pointed out earlier, a space-charge density whic changes rapidly with distance requires smaller volu elements to allow for the correct simulation. Althoug the incremental volume elements are different in var ous parts of the cell, their value in any given region the cell is known. Thus, the only quantities yet und termined at any point are V_s and G, which can be mea ured in the following manner.

The trajectories followed by electrons leaving fro *both* edges of the cathode are plotted out and recorde For large electron beamwidths the cathode is segmente and each segment is treated as the origin of a separat beam. The paths of these two outermost trajectories d fine the boundaries of the electron stream; *i.e.*, all oth electrons that leave the cathode are assumed to trav only between these two boundaries. The beam width a the cathode and at all other points is measured and r corded, thus allowing the calculation of G at every poin

By means of the circuit shown in Fig. 8, the voltag can be measured at every point, with the average of th four voltages being used to represent the potential a the center of the four-probe setup. Of course, with a fiv probe system, as shown in Fig. 4, the potential would b directly measured by the fifth probe, which is pos tioned at the center of the system. In either case, th carriage is manually moved across the cell and the vol age above each source is measured and recorded.

From these values of V_s and G, the currents require at each source to simulate the proper space-charge ca be obtained from (6). These calculated currents are the injected into their respective sources by means of th current injection system shown in Fig. 2.

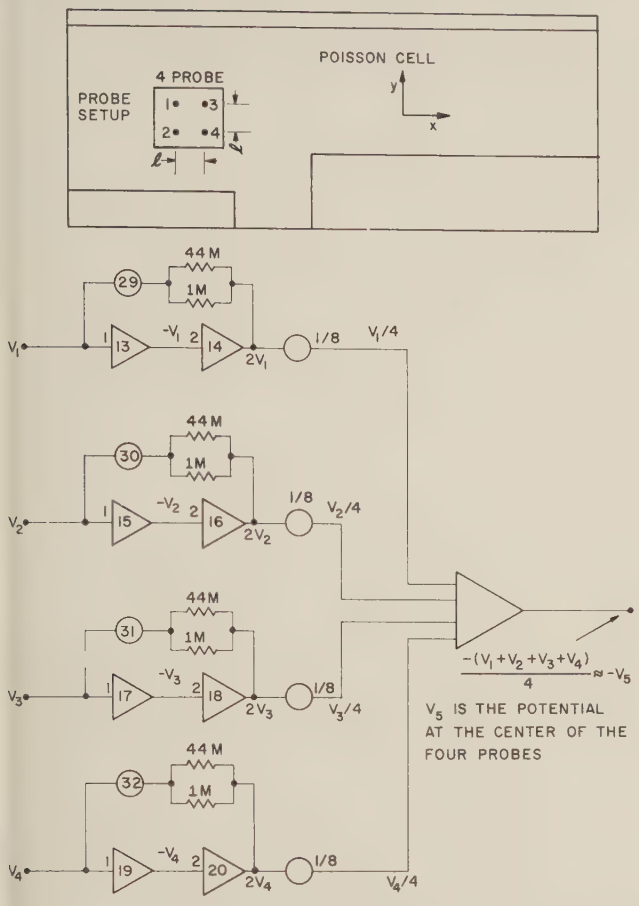


Fig. 8—Potential measurement setup employing four probes and four unloading amplifiers.

The procedure described above is for a four-probe system and although the five-probe method is similar, it has one additional refinement. The amount of space charge at any point in the cell can be obtained from a five-probe system as illustrated in (3).

Now the voltage and distance in the tube are related to the corresponding quantities in the cell by means of constant multiplying factors. Therefore, in terms of cell variables, ρ_t can be written as

$$\rho_t = -\frac{\epsilon_0 F}{l_s^2}(V_{1s} + V_{2s} + V_{3s} + V_{4s} - 4V_{5s}), \quad (7)$$

where F is a constant $= (V_t/V_s)(l_s^2/l_t^2)$.

Eq. (7) shows that ρ_t at any point can be obtained simply by measuring the five potentials. Another expression for ρ_t is given in (5).

In theory the calculations made with (5) and (7) would give the same results for ρ_t. However, in practice the results may be significantly different, since it was assumed in the development of (5) that the cell is completely homogeneous and that the current i_s which is injected into the base of the elementary cylindrical volume element flows toward the top of the cell in such a way that the current flowing radially out of the cylindrical volume is uniform over the surface of the cylinder. In practice, however, there may be inhomogeneities in the cell and since the current tends to diffuse in flowing toward the top surface it is expected that there will be discrepancies between the calculations made using (5) and (7).

To compensate for the above effects, the value of ρ_t must be calculated from (5) and then i_s must be adjusted until the ρ_t measured with the five-point probe system at the top of the cell agrees with the calculations made from (5). This will insure that the proper magnitude of space charge has been simulated.

The rest of the procedure is identical for both the four- and five-probe systems. With currents being injected according to the first set of calculations, the two outermost trajectories are again plotted and recorded. The V_s and G are measured and the entire process repeated to determine the new currents required. After several iterations a set of self-consistent trajectories is obtained, where self-consistent implies that the calculated currents obtained from the V_s and G measurements of two successive runs are exactly the same.

At present all computations and current source settings are being made by hand. Fortunately, the time required is not excessive; a self-consistent set of trajectories is obtainable in one to three days. Nevertheless, the trajectories could be obtained appreciably faster if the calculation and injection of the space-charge simulating currents were performed automatically.

There are several possible ways of automatically determining and injecting the required currents into the Poisson cell to simulate the required space-charge density. The complexity of the equipment needed to accomplish this objective is directly proportional to the degree of accuracy required for the system. The following discussion relates to one of the possible methods. It involves the use of a capacitor bank to store charge proportional to the current to be injected through each source.

The first step would be to partition the cell into square sections, one for each current source, and label these sections. Then the cathode would be divided into an arbitrary number of segments, say M, and the trajectory followed by an electron leaving each sector would be plotted out. This divides the stream into M segments of equal current at the cathode. Since the width of the segments changes along the device, the current density changes from point to point. In order to determine the current to be injected into each current source, a bank of capacitors is arranged with an appropriate switching network so that when the probe carriage passes over a given source a current generator charges the appropriate capacitor in proportion to the time the probe carriage spends over the source. Of course there would have to be a capacitor associated with each current source. It is desired that the capacitors be continuously charged as the trajectories are being

drawn out by the probe carriage. The total charge on each capacitor will then be proportional to the space charge at that point in the cell.

A servomechanism is then used to adjust the space-charge simulating currents using the charge on the individual capacitors as a reference. After the current sources are adjusted for a particular run the capacitors are discharged in readiness for the next run. The flow diagram is shown in Fig. 9.

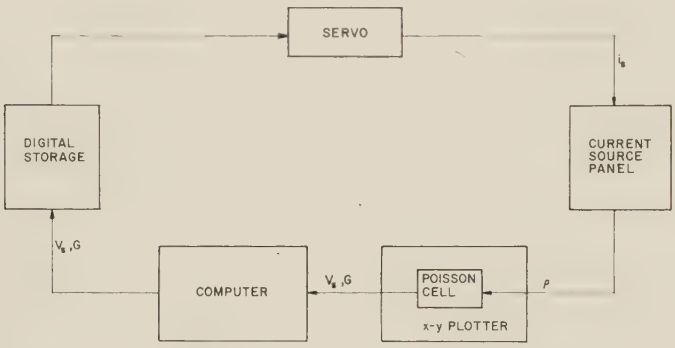


Fig. 9—Flow diagram for automatic current injection system.

There are still other refinements and improvements possible, but each one complicates the problem more and therefore makes it less attractive. The operator must decide what degree of accuracy and complication is really worthwhile.

Other Possible Applications

It was mentioned previously that the Poisson cell has possible application in the solution of all types of potential problems. It also may be used in all areas where two-dimensional nonlinear function generation is a problem. Physical problems of this type are too numerous to list completely at this time.

One possible area of application would be that in which the cell is used as a topographical analog. The equipotential lines in the cell would simulate contours of constant elevation. Hills or valleys could be represented using current injection to change the equipotential distribution at the surface of the cell. Also the rate of change of elevation (gradient) could be easily measured by a probe system on the surface. In this manner any geographical terrain could be effectively simulated.

Conclusions

A solid volume-conducting medium called a Poisson cell has been developed to solve potential problems involving either Laplace's or Poisson's equation. The characteristics of the cell are such that a complete d instrumentation system can be used; hence, the system is free from meniscus errors, polarization effects, and time-varying conductivity effects. It has been shown how the cell may be used in solving a wide variety o problems. In general it can be applied to any problem in fluid flow, electric potential or heat conduction.

In particular the Poisson cell has been applied to the design of electron injection systems, and a procedure has been developed to obtain a set of self-consisten solutions to Poisson's equation. The static and dynamic accuracy of the system using a Poisson cell and an analog computer has been investigated and the over-al accuracy found to be approximately two per cent.

A New, Solid-State, Nonlinear Analog Component*

L. D. KOVACH†, member, ire, and W. COMLEY†

Summary—Since the inception of the electronic analog computer as a useful engineering tool, the need for practical methods of solving nonlinear problems has steadily increased. This paper describes a passive, nonlinear device which, when used with operational amplifiers, provides the means for obtaining a large class of functions. These are obtained to a degree of accuracy and reliability not previously possible with a simple, economical device. A basic varistor squaring unit is described. The unit has been compensated for the various types of error inherent in the varistor itself, and is capable of providing approximately fifteen of the most basic and commonly used nonlinear functions.

* Received by the PGEC, May 20, 1960.
† Engineering Computing Group, Douglas Aircraft Co., El Segundo, Calif.

Introduction

In an ordinary resistor the current is proportional to the voltage across the resistor, the constant of proportionality being the reciprocal of the resistance as exemplified in Ohm's law. For a varistor, however, the relation is

$$I = ke^n. \tag{1}$$

This nonlinear relationship has intrigued many research workers. By far, the majority of these worked on multipliers, taking advantage of the varistor's ability to square a voltage, and making use of the so-called "quar

r-square" identity,[1]

$$1/4[(x+y)^2-(x-y)^2]=xy. \tag{2}$$

he emphasis on multiplication was due to the demand r an economical and stable multiplier and to the fact at the versatility of the varistor for function genera- on had not been recognized.

Work with varistors began at Douglas Aircraft Com- any, El Segundo, Calif., in 1953, and resulted in a aper published in 1954.[2] At that time, the squaring ror was 1.25 per cent of full scale, but only about one aristor in ten met this figure. Because of this and other nitations no further work was done on the multiplier ntil recently. Meanwhile, attention was given to the eneration of various nonlinear transfer functions be- use of the increasing number of nonlinear problems be- g presented for solution. The results of this work were esented at the Second National Simulation Confer- nce in Houston in April, 1957, and published the follow- g year.[3] This last paper stressed the versatility of the aristor but did not report any significant improvement the accuracy.

In 1957, a Russian article[4] described some improve- ents made to the varistor multiplier circuit as well as the title of the 1954 paper.[2] In place of using five nplifiers to perform a multiplication, the Russians had duced this to three and, by an intricate system of vitching, to two. Further investigation showed that by odifying the quarter-square identity, multiplication ould be accomplished with three amplifiers and im- oved accuracy. A new assault was then made on the arious inaccuracies inherent in the silicon carbide aristor. These are 1) inaccuracy of the exponent, 2) a rge negative temperature coefficient, 3) the apparent ability of varistor manufacturers to produce a unit fficiently consistent in its various characteristics, and a slight rectification error. Other objections which ave been raised are the insufficient dynamic range and xcessive insertion loss.

It seems clear that any attempt to build a successful aristor analog computing device must include a recog- tion of the aforementioned difficulties, and must pro- eed systematically to eliminate them one by one.

Description

The basic characteristic of the silicon carbide varistor ven in (1) is repeated here for convenience.

$$I=ke^n. \tag{1}$$

The value of the exponent for commercially available varistors covers a considerable range. The value of n for those most suitable for computer applications is approximately 2.5. If it is desired to generate the square, the exponent n must be made as nearly equal to 2 as possible. This may be accomplished as shown in Fig. 1, the varistor being indicated by R_v. If R is properly determined, the characteristic of the combination is given in

$$I \doteq ke|e|. \tag{3}$$

For each varistor there will be an optimum value of R which most nearly satisfies the relationship given.

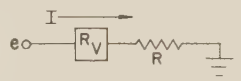


Fig. 1—Modification of the varistor exponent.

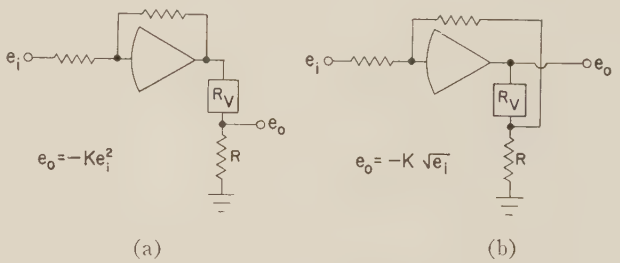


Fig. 2—Basic configurations—single varistor. (a) Square; (b) square root.

Once the varistor has been properly compensated for exponent, there is available a device suitable for generating certain common nonlinear functions. Although many sources of error have yet to be eliminated, the basic configurations are now possible and indicated in Fig. 2(a) and 2(b). While the basic single varistor-resistor combinations shown above are capable of generating the functions given in Fig. 2, there exist a number of undesirable limitations. The most significant of these is the necessity of restricting the input voltage e_i to approximately 8 volts in order to restrict the current through the varistor to a safe value. Excessive current will cause internal temperature changes and result in an undesirable drift. This low input voltage introduces an arbitrary scale factor which is by no means the same for any two varistor-resistor combinations, and in addition results in an insertion loss which tends to restrict the dynamic range of the nonlinear operation. Other disadvantages of the simplified configurations include inconsistency of the error function, *i.e.*, departure from the true square law, and finally, an error of approximately 0.5 per cent due to rectification differences for positive and negative inputs.

The first step in eliminating many of these difficulties may be taken by operating a number of varistors in series. If approximately twelve varistors are used as

[1] This identity had been known for some time, having been found a Louvre tablet dating from about 300 B.C. and appearing con- mporaneously as Proposition 5 of Book II of Euclid's Elements.

[2] L. D. Kovach and W. Comley, "An analog multiplier using yrite," IRE Trans. on Electronic Computers, vol. EC-3, pp. -45; June, 1954.

[3] L. D. Kovach and W. Comley, "Nonlinear transfer functions th thyrite," IRE Trans. on Electronic Computers, vol. EC-7, . 91–97; June, 1958.

[4] A. A. Maslov, "An analog multiplier using thyrite resistors," *utomat. i Telemekh.* (*Automation and Remote Control*), vol. 18, . 336–348; April, 1957.

shown in Fig. 3, the following advantages are obtained: 1) input voltages of 100 volts may now be applied to the circuits shown in Fig. 2 without danger of excessive current, 2) total error is less than for a single varistor unit and the error function is rendered consistent, 3) insertion loss is reduced by a factor of approximately 12 and the dynamic range is correspondingly increased. Moreover, no longer is there dependence on the varistor manufacturer for consistent single units inasmuch as series operation results in an averaging of the characteristics. Larger variations in manufacturing tolerances are compensated for by the number of varistors used. Depending on the characteristics, the number of series units may vary between 10 and 20. For a given production run of varistors, however, the number required has proven to be relatively constant. Fig. 4 indicates a circuit configuration which may now be used to generate a variety of functions.

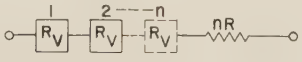


Fig. 3—Series operation of varistors.

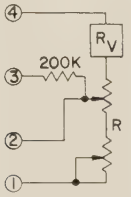


Fig. 4—Generalized configuration.

The potentiometer shown in Fig. 4 makes possible the elimination of arbitrary constants which would otherwise be imposed by variations in varistor characteristics. Combining the improved circuit of Fig. 4 with an operational amplifier, in a manner similar to that shown in Fig. 2, results in a considerable improvement in convenience and accuracy. The circuits shown in Fig. 5 have a basic error not exceeding 0.4 per cent of 100 volts full scale.

Temperature Compensation

A source of error not yet considered, however, is due to the large negative temperature coefficient of the varistors, 0.5 per cent per degree C. This error, fortunately, may be drastically reduced by the proper use of thermistors as shown in Fig. 6.

In Fig. 6(a), for a constant input e_i, e_o will vary as a function of temperature due to the negative coefficient of R_v. The variations may be compensated over a reasonable range of temperature as shown in Fig. 6(b) by substituting a thermistor whose temperature coefficient is equal to, and of the same sign as, R_v. Introduction of the thermistor will maintain a reasonable temperature independence over the range of 55° to 95°F. Operation over

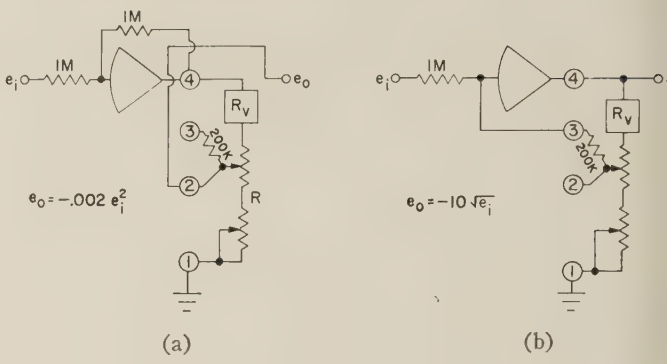


Fig. 5—Basic circuits utilizing the generalized configuration. (a) Square; (b) square root.

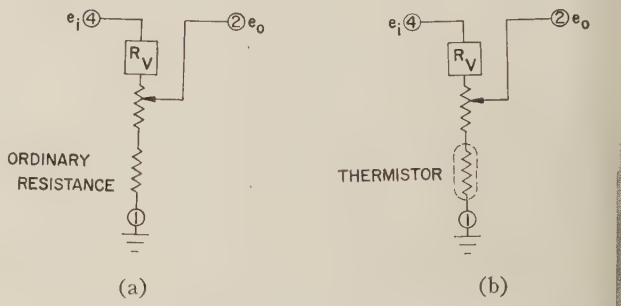


Fig. 6—Temperature compensation. (a) Uncompensated circuit; (b) compensation with a thermistor.

considerably greater ranges may be obtained by enclo ing the unit in a temperature-controlled environmen The small octal-base enclosures used for radio frequenc crystals would be ideal for this purpose.

Rectification Error

One of the disadvantages of the varistor in generatir functions with origin symmetry is the slight rectific tion effect displayed by the material. If a single varist is used to generate such a function, the full scale err due to this effect will vary between zero and 0.6 p cent. Both the General Electric and Globar units di play the same characteristics in this regard.

In constructing the complete unit, this source of err may be eliminated in one of two ways: 1) the fact th a number of varistors are used in series enables the rect fication polarity of each unit to be determined and a units connected so that the polarity of one-half t units opposes the similar effect of the others; 2) if a units are connected without regard to polarity, su rectification error that remains may be eliminated shown in Fig. 7. The resistance R and diode will cau a slight change in the total series resistance. The polari of the diode will depend on the effective polarity of a the varistors in series. In this instance, correction is a complished by reducing K for one polarity of output that it agrees with K for the opposite polarity. Althou both systems are equally effective, a choice will pro ably be determined by economic factors.

A unit embodying all the characteristics previously described has been packaged and given the name "Quadratron."[5] All components are contained in an octal base shield. The unit is shown in Fig. 8.

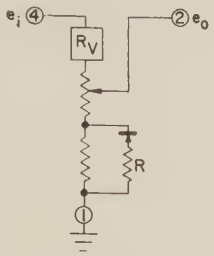


Fig. 7—Elimination of rectification error.

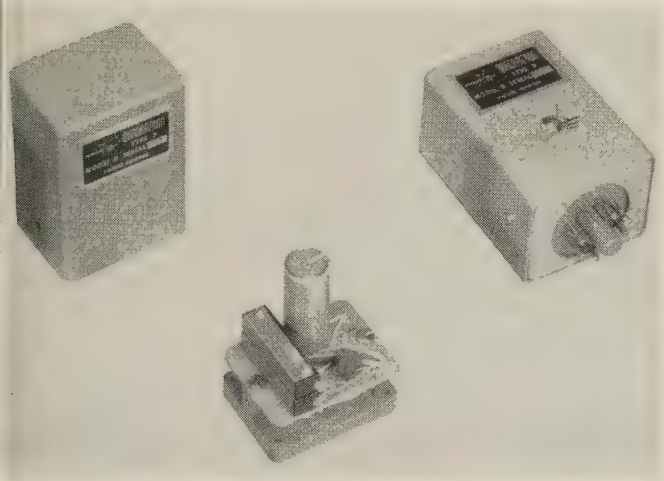


Fig. 8—The Quadratron.

Adjustment and Optimization

In order to obtain optimum results in constructing the Quadratron, two parameters must be correctly determined. These are 1) correct series resistance for exponent adjustment, and 2) correct number of varistors. The circuit diagram, Fig. 9, describes a setup which simultaneously generates two parabolas: one by means of the varistor network (amplifier 4); the other, a reference parabola (amplifiers 1 and 2), by means of two integrations of a constant voltage. The difference of these is taken in a summing amplifier (no. 5) and applied to the Y axis of an oscilloscope. Sweep is provided by means of the ramp available at the output of amplifier 3. The reference parabola is then adjusted so that the sum of the two functions is zero at full scale, *i.e.*, at the end of the sweep. Inasmuch as the reference parabola error may be assumed to be negligible, the pattern on the oscilloscope may be defined as the error function of the varistor squaring device.

[5] From the Latin "quadrare"—to square, and "tron" as in electron."

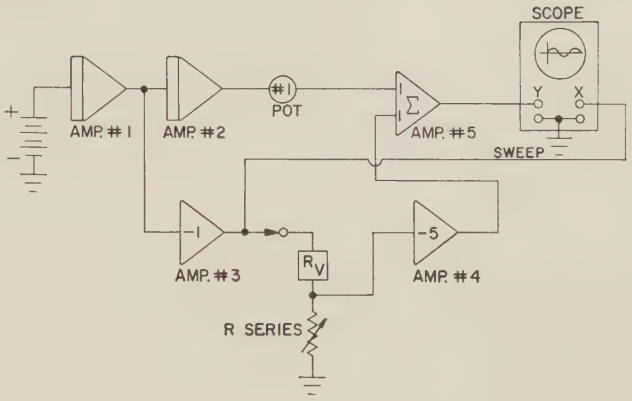


Fig. 9—Circuit for determining varistor parameters.

In order to optimize a particular group of varistors, the first step is to make sure that exactly 100 volts peak is being applied to the varistor network (output of amplifier 3). If the oscilloscope gain is properly adjusted, full scale deflection may be interpreted as 1 per cent error.

The form of the resulting error function provides the clue to the proper adjustment of the series resistance and/or the number of varistors. If both are optimized, the error function will have the appearance shown in Fig. 10.

A reasonable, although arbitrary, starting point is 10 varistors and 8000 ohms. The oscillograms in Fig. 11 will be helpful in determining the correct number of varistors. If for any given number of varistors R is optimized, Fig. 11(a) is characteristic of too few units, 11(b) indicates the correct number, and 11(c) is indicative of too many.

Fig. 12 indicates the effect of varying the resistance when the number of varistors has been optimized. In Fig. 12(a) R is 10 per cent high, in 12(b) R is correct, and in 12(c) R is 10 per cent low.

In varying the parameters, the output of the squaring device will change. This makes it necessary to readjust the reference parabola (potentiometer no. 1) continuously so that the final value of the difference is zero.

The output of the optimized squaring circuit will be between 21 and 25 volts. This enables reduction of the output of all assembled Quadratron units to a uniform 20 volts.

The test circuit is normally arranged to operate on a repetitive basis and at a rate of about 1 cps. This makes it possible to observe the error function continuously, and is not only convenient but essential where parameter variations are involved.

Characteristics of the Quadratron

With the peak input signal of 100 volts, the current required from the driving source will be between 1 and 2 ma. This requirement, together with low source impedance, is easily realized with almost any dc opera-

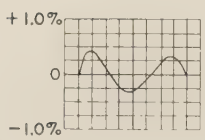


Fig. 10—Typical error curve.

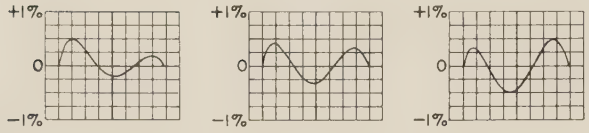


Fig. 11—Variation in error curve with number of varistors. (a) Too few varistors; (b) correct number of varistors; (c) too many varistors.

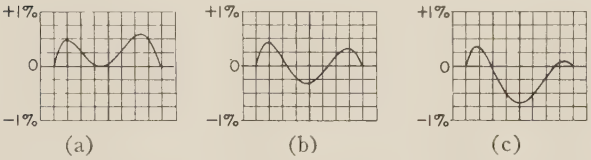


Fig. 12—Variation in error curve with series resistance. (a) Resistance is 10 per cent high; (b) resistance is correct; (c) resistance is 10 per cent low.

tional amplifier. The base diagram of the Quadratron is shown in Fig. 13.

An important consideration in maintaining maximum accuracy is the necessity of operating the unit into the same impedance with which it was calibrated. A value of 200 K ohms was chosen. This value provides a gain of 5 in the basic squaring configuration—the exact gain required to amplify the full scale output of 20 volts to the more useful 100-volt level. For the sake of convenience, a 200-K precision resistor is included in the unit package and may be connected directly to the amplifier summing junction. If the output is taken directly from pin two, an external load of 200 K ohms must be provided.

The bandwidth of the Quadratron is approximately 0–400 cps for functions which may be obtained with the output configuration, *i.e.*, Fig. 5(a); and 0–50 cps for functions utilizing the feedback configuration, *i.e.*, Fig. 5(b). In each case, the upper limit is defined as that point at which phase shift becomes apparent in the Lissajous presentation of input vs output. The bandwidth limitations are due to the capacity of the varistor units shown in Fig. 14. The time constant τ due to R_v and C_{R_v} is dependent upon the input voltage as shown in (4):

$$\tau = \frac{KC_{R_v}}{e_i} . \tag{4}$$

This voltage dependence of the time constant complicates the problem of providing frequency compensation. At the present time, however, work is under way to

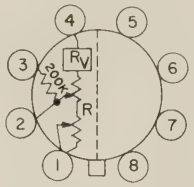


Fig. 13—Quadratron base diagram.

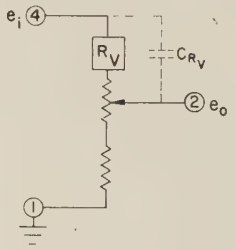


Fig. 14—Parasitic capacitance of varistors.

determine the feasibility of using nonlinear silicon capacitors to extend the usable bandwidth.

Some drift of the Quadratron output will be noted in cases where a high input voltage is applied continuously. This effect can amount to as much as 1 per cent when 100 volts is applied over a prolonged period. This drift decreases approximately as the square of the mean continuous input signal level, and becomes negligible for normal operation. For those applications where a large dc bias voltage is present in the input signal, a 20 minute warm-up period should be allowed for stabilization of the drift before circuit calibration is attempted. The multiplier, Fig. 17, is a typical example of this type of application.

Applications

The methods by which a squaring device may be used to generate a variety of useful nonlinear functions are by no means apparent. In addition to the square and square root, which have already been mentioned, many other useful functions may be obtained. Much of this versatility stems from the fact that the Quadratron displays origin symmetry, rather than axis symmetry in the generation of the square. This characteristic is expressed in (5) for the basic squaring operation:

$$e_0 = Ke_i \left| e_i \right| . \tag{5}$$

The axis symmetry required of the true square may, of course, be obtained by applying the absolute value of the input variable in (5). In other instances, however, the origin symmetry characteristic will be of great value. Many of the applications to be discussed in this section are a straightforward utilization of the square. Others are obtained by means of new and unique algebraic approximations which have been devised not only for accuracy but ease of mechanization.

Fig. 15(a) shows the basic squaring operation having origin symmetry. Maximum accuracy will be ob

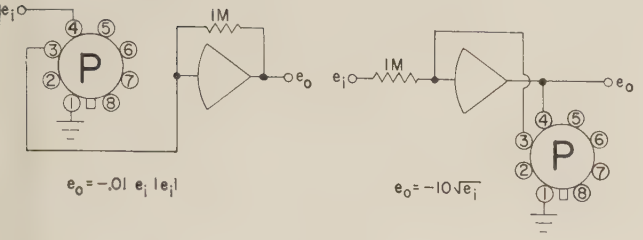


Fig. 15—Basic Quadratron circuits. (a) Squaring with origin symmetry; (b) square root.

lined with an input of 100 volts peak. This configuration is particularly useful for representing square law amping terms. Circuits of this type may be cascaded give exponents of 4, 8, etc. The fourth power is valuble in representing the radiation terms in heat transr problems. The symmetrical or true mathematical uare can be generated by means of the same basic uaring circuit. In this case, the absolute value of the put voltage must be applied.

By placing the Quadratron in the feedback of the erational amplifier, the square root of an input voltage ay be obtained as shown in Fig. 15(b). The square ots of negative voltages will also be obtained as negave voltages but these can be blocked by diodes if dred.

The operations described above may be combined as own in Fig. 16. This configuration provides the solun of the right triangle. It may also be considered as a eans of obtaining the proper sum of perpendicular ectors. It is a mechanization of the equation $e_0 = K\sqrt{e_1^2+e_2^2}$. In this case the voltage limitation on the puts is 70 volts peak. This circuit has application in ophysics, vector resolution, coordinate transformaon, statistics, etc. Perhaps no other application of the uadratron illustrates so well the possible reduction of quipment and the attendant gain in reliability as this ne.

Multiplication is achieved by the use of a unique varition on the well-known quarter square identity. This volves the addition of a constant term which yields

$$(x - y - K)^2 - (x + y + K)^2 + 4Kx = -4xy, \quad (6)$$

here $|x| + |y| \leqq K$. The circuit constants in Fig. 17 ave been carefully chosen to provide optimum results r inputs of ± 100 volts peak. In order to obtain maxium accuracy, the resistors in the input and feedback the input amplifiers should be on the order of 0.1 per nt of the indicated values. The adjustment procedure as follows:

1) Ground e_i, apply 100 volts-dc to e_2, adjust ① for zero output.
2) Ground e_2, apply 100 volts-dc to e_1, adjust ② for zero output.
3) 100 volts-dc to e_1 and e_2, adjust ③ for 100 volts output.

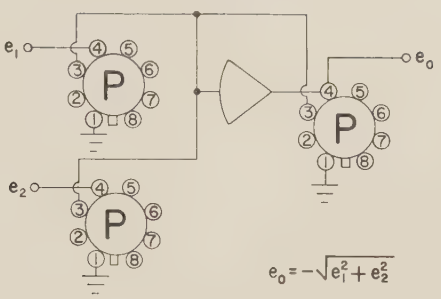


Fig. 16—Square root of a sum of squares.

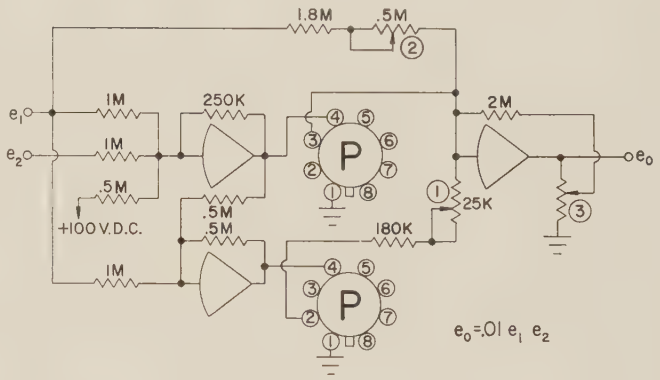


Fig. 17—Multiplication circuit.

The frequency response of this circuit is excellent. For optimum results, however, capacitive equalization of some of the amplifier input resistors may be required. Division may be performed by using the identity

$$\frac{x}{z} = (1 - z)\frac{x}{z} + x, \quad (7)$$

which may be mechanized with only slight modification of the multiplier circuit. In order to maintain good stability, the denominator voltage is usually confined to the range $-100 \leq z \leq -5$.

A circuit yielding $e_0 = Ke_i^N \operatorname{sgn} e_i$ is shown in Fig. 18. (Note: $\operatorname{sgn} x = x/|x|$.) The novelty of this arrangement lies in the fact that N is continuously adjustable between the values of $\frac{1}{2}$ and 2. Adjustment is obtained by means of a potentiometer capable of including any desired part of the Quadratron output inside the amplifier feedback loop. Depending upon the setting, a partial linearization of the Quadratron results in an output voltage with the required degree of nonlinearity.

A unique method of generating the sine is shown in Fig. 19. The mechanization of the equation

$$\sin e_i = Ay - By^2 \operatorname{sgn} y, \quad (8)$$

where

$$y = \pi e_i - e_i^2 \operatorname{sgn} e_i, \quad (9)$$

results in an approximation of $\sin e_i (-\pi \leq e_i \leq \pi)$ with an error less than 0.09 per cent of full scale.

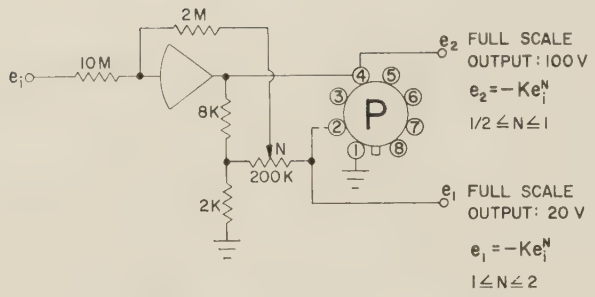


Fig. 18—Adjustable exponent.

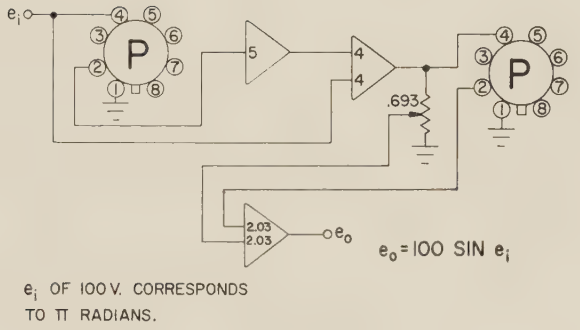


Fig. 19—Sine function.

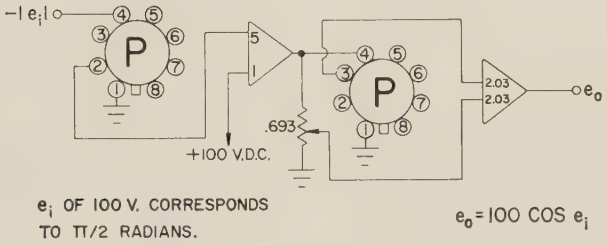


Fig. 20—Cosine function.

Fig. 20 shows a method of generating an approximation for $\cos e_i (-\pi/2 \leq e_i \leq \pi/2)$. The method consists of modifying (8) and (9) to

$$\cos e_i = Ay + By^2, \tag{10}$$

where

$$y = \left(\frac{\pi^2}{4} - e_i^2\right). \tag{11}$$

In order to extend the range of e_i, the angle may be doubled by means of the trigonometric identity

$$\cos 2x = 2\cos^2 x - 1. \tag{12}$$

A further illustration of the versatility of the Quadratron is afforded by the unique method used to represent the tangent function. The expression

$$\tan e_i = 1.091e_i - 0.176e_i^2 \operatorname{sgn} e_i + 0.651e_i^4 \operatorname{sgn} e_i \tag{13}$$

represents the tangent in the interval $-\pi/3 \leq e_i \leq \pi/3$,

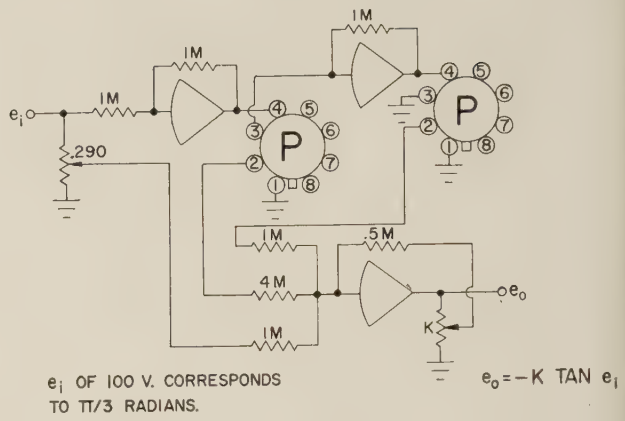


Fig. 21—Tangent function.

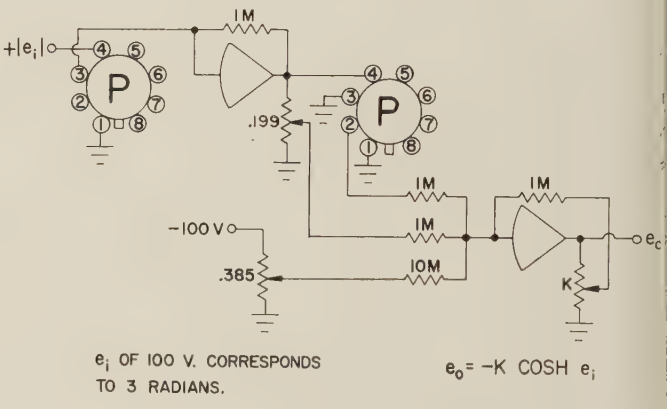


Fig. 22—Hyperbolic cosine function.

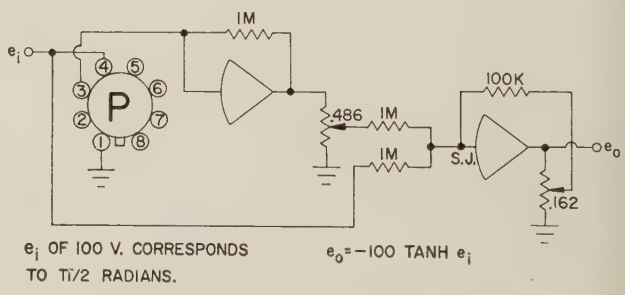


Fig. 23—Hyperbolic tangent function.

with an error less than 0.55 per cent of full scale. Not that only squaring operations are required in the circui shown in Fig. 21. A gain adjustment in the final sum ming amplifier will provide the appropriate scaling.

A hyperbolic cosine function may be obtained b means of the circuit shown in Fig. 22. It utilizes a trun cated series of only three terms. The absolute value c the input variable must be provided.

A truncated series consisting of only two terms ma be used to represent the hyperbolic tangent in the inter val $-\pi/2 \leq e_i \leq \pi/2$. The error of this approximation i on the order of 0.5 per cent of full scale. Fig. 23 shows th necessary circuit for obtaining the function.

Several other interesting applications have been und which, although not directly related to nonlinear mputation, have proven nonetheless useful.

Transducers displaying troublesome nonlinearities ve been successfully linearized by introducing into e system the required degree of complementary non-earity. The square and square root circuits have en used to provide compression and expansion in strumentation systems, and a highly successful ase-sensitive modulator, Fig. 24, has been designed. his unit is a modification of the multiplication scheme scribed previously. Because of the less stringent filter quirements, it displays a considerably improved band-idth characteristic over units utilizing the conven-onal diode switching method.

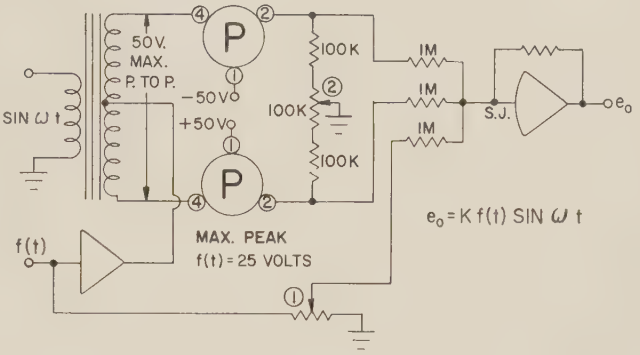


Fig. 24—Phase-sensitive modulator.

Conclusion

The Quadratron is a reliable, simple, versatile, eco-omical device for generating a large number of non-ear functions. Its building block simplicity makes it ossible for the design engineer to gain new insight into the behavior of nonlinear systems. The ability to square leads to a number of interesting and unusual techniques for performing difficult nonlinear jobs.

Acknowledgment

The authors wish to express their appreciation to M. F. Williams for his design of the phase-sensitive modulator.

Solving Integral Equations on a Repetitive Differential Analyzer*

R. TOMOVIĆ† and N. PAREZANOVIĆ†

Summary—**Methods of practical solution of integral equations on ectronic differential analyzers are not well developed. In those cases here such methods have been outlined, special and costly addi-onal equipment is required.**

Results presented in this work show that practical solution of tegral equations is possible using a repetitive differential analyzer convenient design.

Introduction

THE application of analog computers to the solution of one-dimensional problems in mathematical analysis is well established today. Differential analyzers have become standard tools in the solution of oth linear and nonlinear equations.

The solution of two-dimensional problems on an elec-onic differential analyzer involves some obvious diffi-ulties. There is no direct way to represent two or more independent variables on the electronic analyzer. However, because of the good frequency response of electronic computing elements, the principle of scanning can be used to treat two-dimensional problems on repetitive differential analyzers.[1]

In this paper, attention will be directed to the practical solution of integral equations on repetitive computers. It is interesting that although integral equations attracted the interest of workers in the analog field quite early, few practical results have been published. In those cases where practical results are available, it is necessary to add complex auxiliary equipment to the existing computer.

When a suitable general-purpose repetitive differential analyzer is at one's disposal, however, solutions of integral equations can be obtained with sufficient speed and with no additional equipment.

* Received by the PGEC, March 6, 1960; revised manuscript ceived, August 16, 1960.

† "Boris Kidrich" Institute of Nuclear Sciences, Belgrade, Yugo-avia.

[1] R. Tomović, "Calculateurs Analogiques Répétitifs," Masson et Cie, Paris, France; 1958.

Fredholm's Equation of the Second Kind

Let us take Fredholm's integral equation of the second kind,

$$y(x) = f(x) + \lambda \int_a^b K(x, t) \cdot y(t)dt \qquad (1)$$

where $f(x)$ and the kernel $K(x, t)$ are given. Since there is no interest in general methods of obtaining the solution of (1), only principles appropriate for analog computers will be considered. Other problems encountered in the application of analog computers, such as generation of the kernel $K(x, t)$ will be treated later in the text.

Mathematically speaking, all proposals concerning analog solution of integral equations were based on the method of successive approximations and quantization of the kernel $K(x, t)$ in the variable x into k steps. The method of transforming the integral equation into a set of algebraic equations and then solving it on an analog computer cannot be considered a pure analog procedure.

An early proposal to solve integral equations on an analog computer was made by Wallman.[2] His paper was primarily concerned with integral equations of the first kind,

$$F(x) = \int_a^b K(x, t) \cdot y(t)dt, \quad F(x) \text{ given.}$$

A repetitive analog computer had the role of performing the necessary integrations in an iteration process starting with $y = y_0(t)$. The variable x was quantized into k steps. Otherwise the classical mathematical iteration procedure was not modified.

A much faster iteration process, adapted to analog techniques, was proposed by Fisher.[3] This method was applied to (1) and can be written as

$$y_n(x) = f(x) + \lambda \int_a^{x-(1/2)\Delta x} K(x, t)y_n(t)dt + \lambda \int_{x-(1/2)\Delta x}^b K(x, t) \cdot y_{n-1}(t)dt \quad \Delta x = \frac{b - a}{k}.$$

In the classic iteration method, the term $y_n(t)$ on the right-hand side is replaced by $y_{n-1}(t)$ so that the estimate for $y(t)$ is not improved until $y_{n-1}(x)$ has been computed for all x_i; while in Fisher's process, after each individual change in x_i, the function $y_n(t)$ is continuously adjusted for a better approximation.

In our work Fisher's iteration procedure was utilized as mathematical background. However, as proposed in its original form, Fisher's method requires an analog memory and other equipment that has to be designed for this specific purpose and has not been available commercially.

Results presented in this paper were obtained on the repetitive differential analyzer of the Institute "Boris Kidrich" without any additional equipment.[4] Thus a further step in the practical solution of integral equations has been achieved.

The application of the above repetitive differential analyzer to the solution of (1) is quite straightforward. Let us take

$$y(x) = \frac{3x}{2} - \frac{7}{6} + \int_0^1 (x - t) \cdot y(t)dt, \qquad (2)$$

the solution of which is

$$y(x) = x - 1.$$

The analog network of (2) is given in Fig. 1. The repetition rate of the analyzer used was 50 cps.

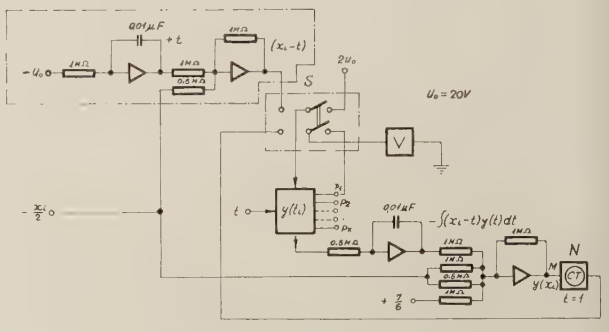


Fig. 1—Analog network for the solution of integral equation (2). Points p_i represent taps of potentiometers on which each ordinate $y(t_i)$ is set as a dc voltage. When the corresponding dc level $y(t_i)$ is being adjusted by use of a voltmeter, the set of function generator potentiometers is supplied by chosen unit voltage u_0. Normally the potentiometers are supplied with variable voltage $x_i - t$ as indicated by switch S. N is a measuring system including sampling and hold circuit.

The function generator simultaneously performs the multiplications[5] giving a step output. Each ordinate $y(t_i)$ can be individually adjusted without any influence on successive function values.

Integrals of the form

$$\int_0^t (x_i - \tau)y(\tau)d\tau$$

for each $x = x_i$ are displayed on the screen of the cathode ray tube. At the same time the operator can measure any instantaneous value $t = t_i$ within the limits of integration.

Applications of Fisher's iteration method are now quite easy. In the first integration $x = x_1$ and $y_1(t) =$

[2] H. Wallman, "An electronic integral-transform computer and practical solution of integral equations," *J. Franklin Inst.*, vol. 250, pp. 45–61; January, 1950.

[3] M. E. Fisher, "On the continuous solution of integral equations by an electronic analogue," *Proc. Cambridge Phil. Soc.*, vol. 53, pt. 1, pp. 162–174; 1957.

[4] R. Tomović and D. Mitrović, "Some experiences with a repetitive differential analyzer," *Bull. Inst. "Boris Kidrich,"* vol. 8, pp. 109–116; March, 1958.

[5] R. Tomović, "A versatile electronic function generator," *Franklin Inst.*, vol. 257, pp. 109–120; February, 1954.

e used. The operator then measures the value of the ght side of (2) for $t=1$ at point M. This value is obined as a dc voltage with the aid of a sample-and-ld circuit that is part of the measuring system. Thus e first ordinate $y_2(x_1)$ is obtained.

Using switch S, the dc voltage corresponding to $y_2(x_1)$ set on the first potentiometer of the function genator. Thus the second minor iteration cycle starts with

$$y(t) = y_2(t_1) \qquad t \leqq t_1 + \Delta t$$
$$y(t) = y_1(t) \qquad t > t_1 + \Delta t.$$

t the next step, the operator uses $x=x_2$ and repeats the easurement at $t=1$. The second ordinate $y_2(x_2)$ is now ailable, and so on.

After k minor iteration cycles, the whole function (x) is at one's disposal. The major iteration cycle may w be repeated, but practical experience has shown at no more than two major iteration cycles, $y(x)$ $y_3(x)$, are ever needed. Fig. 2 represents the differenal analyzer solution of (2) obtained after two major eration cycles. The number of ordinates $y(x_i)$ was =16. The time taken to arrive at the final solution was out five minutes.

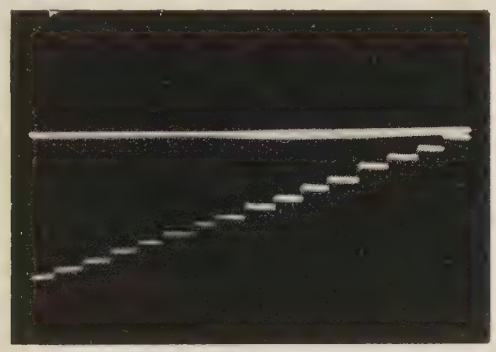


Fig. 2—Solution of integral equation (2) as obtained on the repetitive differential analyzer.

Volterra's Equation of the Second Kind

Integral equations with variable upper limit

$$y(x) = f(x) + \lambda \int_a^x K(x, t) \cdot y(t) dt \tag{3}$$

e solved in the same way. Actually the solution of (3) obtained in k independent adjustments. Namely, (3) n be approximated in the following way:

$$y(x_i) = f(x_i) + \lambda \int_a^{x_1} K(x_i, t) \cdot y(t_1) dt + \lambda \int_{x_1}^{x_2} K(x_i, t) \cdot y(t_2) dt + \cdots + \lambda \int_{x_{i-1}}^{x_i} K(x_i, t) \cdot y(t_i) dt.$$

The number of steps k corresponds to the number of ordinates $y(t_i)$, $i=1, 2, \cdots, k$. In the first phase, the iteration procedure is applied to x_1, as follows:

$$y(x_1) = f(x_1) + \lambda \int_a^{x_1} K(x_1, t) \cdot y(t_1) dt.$$

Measurement of the instantaneous value of $y(t)$ is now performed at $t=t_1$. In two iterations each value of $y(t_i)$ is practically always obtained.

In the second phase,

$$y(x_2) = f(x_2) + \lambda \int_a^{x_1} K(x_2, t) y(t_1) dt + \lambda \int_{x_1}^{x_2} K(x_2, t) \cdot y(t_2) dt$$

is solved on the computer. The variable t is measured at $t=t_2$ and $y(t_2)$ set on the function generator. The method of computing successive values of $y(t_i)$ is now evident. Individual ordinates $y(t_i)$ are obtained in independent iteration cycles.

As an example, the following integral equation was solved on the differential analyzer:

$$y(x) = 3x + \int_0^x Sh(x - t) \cdot y(t) dt. \tag{4}$$

Its solution is

$$y(x) = \frac{3x}{2} + \frac{3\sqrt{2}}{2} Sh(x\sqrt{2}).$$

The kernel $Sh(x-t)$ was generated by subtracting two exponentials, each of which was computed as the solution of a differential equation. Namely, $Z_1 = e^{(x-t)}$ is the solution of

$$\frac{dz_1}{dt} + z_1 = 0 \quad \text{with} \quad z_1(0) = e^x,$$

and $Z_2 = e^{-(x-t)}$ is the solution of

$$\frac{dz_2}{dt} + z_1 = 0 \quad \text{with} \quad z_2(0) = e^{-x}.$$

The part of the analog network which generates $Sh(x-t)$ is surrounded by broken lines in Fig. 3.

The solution of (4) is seen in Fig. 4. The number of ordinates taken was $k=16$. Maximum error at the end of integration interval was 5 per cent.

Limitations of the Method

Theoretical limitations

Thus far it has been supposed that kernel $K(x, t)$ can be decomposed into a combination of two functions of one independent variable each, $f(x)$ and $f(t)$. In many practical cases this assumption holds, for instance, when $K(x, t) = K(x-t)$. Besides, there are other ways to avoid a two-variable function generator.[3]

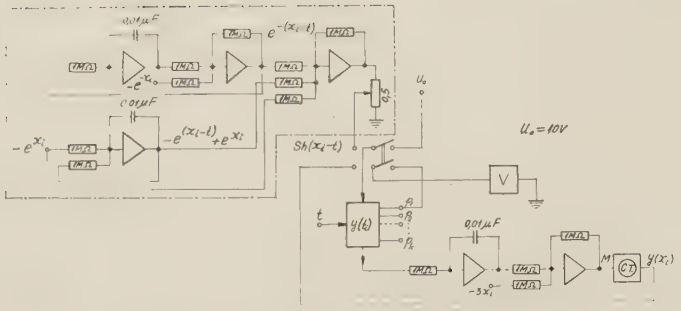


Fig. 3—Analog network for the solution of integral equation (4).

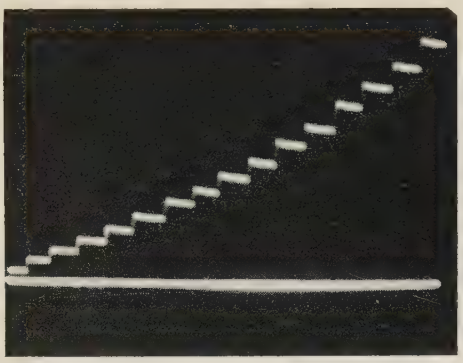


Fig. 4—Solution of integral equation (4).

In the light of this research work, the paper by Moon and Spencer[6] is of special interest. Studying errors in integral equations due to kernel approximation by exponential and other simpler expressions, they have stressed the fact that in engineering applications such simplifying assumptions are justified. In conclusion, it can be stated that a two-variable function generator is not really needed for solving integral equations. Direct generation of $f(x)$ and $f(t)$ covers practical applications.

In the original considerations, the number of steps k taken was of the order of 100.[2] Later work[3] pointed out, and our results confirmed, that the kernel $k(x, t)$ has a high degree of "redundancy," and that quantization of x into 15 to 30 steps is most frequently sufficient for engineering applications.

Equipment

As may have been noticed, full attention was given in this paper to solving integral equations on conventional differential analyzers without introducing special equipment. Indeed, no such equipment was used except that the following requirements concerning some nonlinear computing elements and the measuring system had to be met:

a) The function generator must allow individual adjustment of each ordinate without any mutual interference if convergence of the iteration process is to be assured.
b) The measuring system must be provided with circuits permitting the measurement of instantaneous values of wave forms.
c) It is desirable to have the function generator as a universal nonlinear unit in order to perform multiplication within the same element. This considerably simplifies the analog network.

Repetitive differential analyzers fulfilling the above requirements are easily prepared and are even commercially available. With some additional simple equipment the solutions of integral equations can be obtained even more quickly should it be necessary.

Conclusion

The field of practical solution of integral equations by differential analyzers has not yet been fully explored. The possibility of using differential analyzers in this application provides a basis for future work in solving concrete problems in engineering and science. A list of such problems has already been presented.[2] We refer particularly to applications in the study of feedback systems with easy transfer from time to frequency domain and vice versa.

On the other hand, this work shows the wide possibilities of repetitive differential analyzers. Solution of differential equations, linear and nonlinear, and synthesis problems is already well established. Recently, a direct and elegant method for finding real and complex roots of polynomial equations by the use of a repetitive differential analyzer has been presented.[7] Integral equations can also be handled in a straight-forward way.

The repetitive differential analyzer is thus a very general and useful piece of equipment for analog computing centers. Naturally, it cannot replace large analog installations of high precision, because of its limitations in drift and accuracy.[8] But for problems of moderate size for smaller laboratories and computing centers, or as additional equipment to other computers, its place rank higher than it would seem at first sight. The general field of application of the repetitive analyzer is of very great value for teaching purposes where relatively simple and inexpensive equipment with diversified application is highly desirable.

[6] P. Moon and D. E. Spencer, "Errors in the solution of integral equations," *J. Franklin Inst.*, vol. 264, pp. 29–41; January, 1957.

[7] P. Madić, J. Petrić, and N. Parezanović, "The use of a repetitive differential analyzer for finding roots of polynomial equations," IRE Trans. on Electronic Computers, vol. EC-8, pp. 182–185; June, 1959.

[8] R. Tomović, "The Role of the Repetitive Differential Analyzer," presented at Automation Congress, Madrid, Spain; October, 1958.

A New Technique for Analog Integration and Differentiation*

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Summary—A technique is described which enables an approach ideal analog integration or differentiation by means of passive ents only. A series of RC circuits in a cascade arrangement, pupled to each other, provides the first, second, third, etc., inte- s or derivatives (according to the connection of the RC circuits) he input function. The theory establishes that if the outputs of are fed to an analog summing amplifier, its output becomes trarily close to the ideal integral or derivative of the input func- as the number of RC stages is raised indefinitely. A device has developed according to this idea to perform one of these ations (integration) and to check the results obtained in theory. hematical proofs of the theory are given in the paper.

Introduction

ANALOG differentiation or integration is based upon basic RC circuits connected in each case according to the corresponding use. They can give wable results only for relatively short computing ervals of time. In order to extend their performance, ve elements have been introduced in many ways ., amplifiers). This investigation presents the possi- ty of approaching ideal integration or differentia- without voltage amplifiers. Only RC circuits and al devices with special characteristics as defined ow are used. The purpose of these elements is to de- ple the RC circuits connected in cascade. In the ctical example, impedance decoupling elements such cathode followers have been used as practical ap- aches to the elements required in the theory.

General Description

ig. 1 is a schematic diagram of an ideal circuit, de- ped according to the mathematical pattern of the ory. The blocks named S have the following char- eristics: input impedance $= \infty$, output impedance , voltage transfer $= 1$. A series of RC circuits with S ents placed in between are connected in a cascade ngement. In this particular case, the RC connection esponds to analog integration.

he signals obtained from the capacitor nodes are to the summing device Σ. Its output $e_0(t)$ is an ap- ximate integral function of the input signal $e_i(t)$. output voltage $e_0(t)$ differs from the ideal integral ction of $e_i(t)$ for two reasons: 1) the summing device ot a perfect one, though it can be improved without t; 2) the number of RC-S stages is not infinite;

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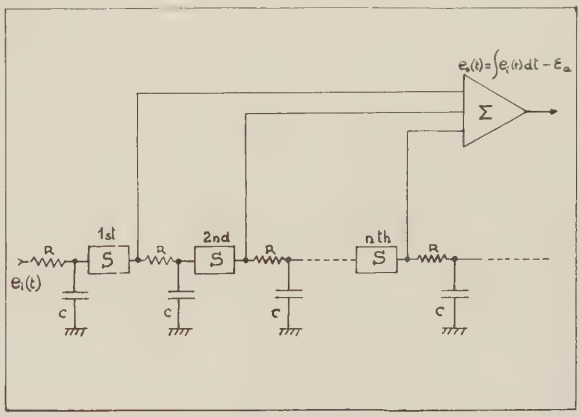


Fig. 1—Schematic diagram of a cascade-integrating circuit with RC stages and decoupling elements s connected in between. The outputs of the RC circuits are fed to an analog summing device Σ.

nevertheless, it can be increased without limit, at least in theory.

Before giving a rigorous demonstration, we can visualize the phenomena through an intuitive description according to the following line of thought. The first RC-S stage gives a voltage that approximates $\int e_i(t)dt$ to a degree dependent on t/τ, where t is the computation-time interval, and τ is the time constant of the RC circuit. This approximation obtains with an absolute negative error for any value of t. If in any instant we add to that voltage the necessary amount to make that error vanish, we obtain just the true integral function. That is exactly what happens in the summing circuit when the number of stages (RC-S) is raised indefinitely.

In other words, the absolute negative error of voltage obtained for an analog integral function in a cascaded RC-S circuit of indefinitely large extent is equal to the sum of the voltages obtained from all the following RC stages. The same considerations can be applied to a derivative-computing device developed according to the same pattern.

Mathematical Proofs

The transfer function in the Laplace domain corresponding to an RC-S stage is

$$\frac{1}{1+s\tau}.$$

The signals obtained in each of the node capacitators corresponding to an input of Laplace transform $e_i(s)$ are:

$$\text{first stage} \quad \frac{e_i(s)}{1 + s\tau},$$

$$\text{second stage} \quad \frac{e_i(s)}{(1 + s\tau)^2},$$

$$n\text{th stage} \quad \frac{e_i(s)}{(1 + s\tau)^n}.$$

The sum of this voltage transformed for n stages is

$$e_0(s) = e_i(s)\left[\frac{1}{1 + s\tau} + \frac{1}{(1 + s\tau)^2} + \cdots + \frac{1}{(1 + s\tau)^n}\right].$$

Evaluation of the sum yields

$$e_0(s) = e_i(s)\left[\frac{1}{1 + s\tau} \cdot \frac{\dfrac{1}{(1 + s\tau)^n} - 1}{\dfrac{1}{1 + s\tau} - 1}\right].$$

It is convenient to write it as follows:

$$e_0(s) = \frac{e_i(s)}{s\tau} - \frac{e_i(s)}{s\tau(1 + s\tau)^n}.$$

$e_0(s)$ is then formed by two terms: 1) the exact integral function of the input; 2) the negative error inherent to the method. It follows immediately that the error term becomes arbitrarily close to zero as n is raised arbitrarily, so that $e_0(s)$ becomes the perfect integral of the input.

It is possible to differentiate functions following the same general pattern used for integration, substituting RC differentiators for the RC integrators, in the diagram of Fig. 1. The output voltage is then:

$$e_0(s) = e_i(s)s\tau - e_i(s)s\tau\left(\frac{s\tau}{1 + s\tau}\right)^n.$$

As in the integration case, $e_0(s)$ is formed by tw terms: 1) an ideal derivative of the input function; 2) negative error inherent to the method. When n is raise arbitrarily, the last term becomes arbitrarily close zero. It follows that in the limit, $e_0(s)$ becomes the deri ative of the input function.

In the laboratory the method was checked with three-stage integrator and an input-step function $e_i($ $= E$. The expected errors were previously calculated f 1, 2, 3, and 4 integrating stages. The absolute error voltage ϵ_a was calculated from the inverse Lapla transform of

$$-\frac{e_i(s)}{s\tau(1 + s\tau)^n},$$

with $e_i(s)$ replaced by $1/s$ (thus setting $E=1$). Letti $t/\tau = k$, the results are:

$$n = 1: \ \epsilon_a = -e^{-k} + 1 - k,$$

$$n = 2: \ \epsilon_a = -e^{-k}(2 + k) + 2 - k,$$

$$n = 3: \ \epsilon_a = -e^{-k}\left(3 + 2k + \frac{k^2}{2!}\right) + 3 - k,$$

$$n = 4: \ \epsilon_a = -e^{-k}\left(4 + 3k + 2\frac{k^2}{2!} + \frac{k^3}{3!}\right) + 4 - k.$$

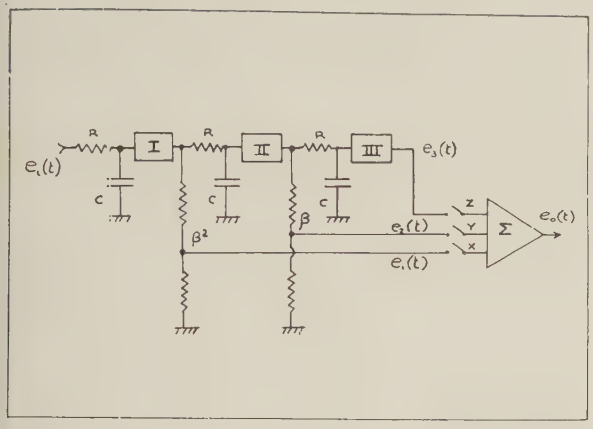
From the equations we can induce a general formula f the absolute error ϵ_a that will result from integrating unit step of voltage in a cascade of n RC-S circuits,

$$\epsilon_a = -e^{-k}\left[n + (n-1)k + (n-2)\frac{k^2}{2!} + \cdots + \frac{k^{n-1}}{(n-1)!}\right] + n -$$

Giving values to k we obtain Table I, in which the pe centage error has been calculated from $\epsilon_a/k \times 100$, b cause $k = t/\tau$ is the exact integral of a unit-step inpu

TABLE I

	n	$K = t/\tau$							
		1	2	3	4	5	6	7	8
Absolute Errors	1	−0.37	−1.14	−2.05	−3	−4	−5	−6	−7
	2	−0.10	−0.54	−1.25	−2.12	−3.03	−4	−5	−6
	3	−0.04	−0.22	−0.68	−1.35	−2.17	−3.08	−4	−5
	4	−0.02	−0.07	−0.33	−0.85	−1.43	−2.23	−3.12	−4.04
Percentage Errors	1	37	57	68	75	80	83	86	87
	2	10	27	42	53	61	67	71	75
	3	4	11	23	34	43	51	57	62
	4	2	3.5	16	21	29	37	44	50



g. 2—Three RC integrators circuits with three cathode followers I, II, and III, and the attenuators β^2 and β used to compensate for the corresponding slight voltage attenuations of II·III and III respectively.

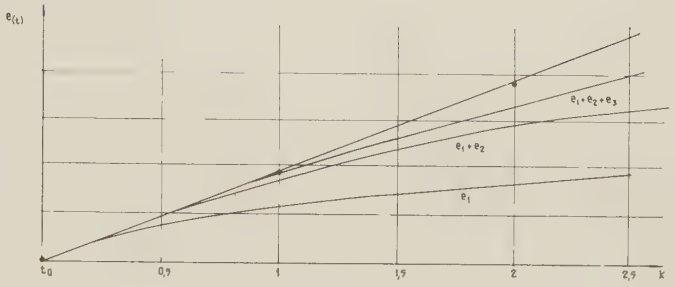


Fig. 3—Output voltages e_1, e_1+e_2, and $e_1+e_2+e_3$ corresponding to the circuit of Fig. 2. The straight line corresponds to the ideal integration that should be obtained with $N=\infty$.

Circuit

The experimental circuit shown in Fig. 2 includes ree RC integrators and uses three cathode followers buffer elements. A cathode follower was used, since it a circuit that approximates the requirements of the eory.

The signals fed to the summing device from Stages I d II have been attenuated by β^2 and β to compensate e corresponding attenuations of II·III and III re-ectively. By means of switches x, y, and z, we can se-ct and record the output signals e_1, e_1+e_2, and e_1 e_2+e_3, corresponding to $n=1, 2, 3$. The ideal integral the input-step function was superimposed on the same aph of Fig. 3 by drawing a straight line of slope E/τ through the origin. A check of the error calculations was made by plotting in Fig. 3 the points corresponding to $k=1$ and $k=2$ for the exponential $e_1+e_2+e_3(n=3)$, using the experimental data plus the magnitude of the error term as given in Table I.

The use of electron tube cathode followers is not considered to be an essential part of the method. Any suitable decoupling device may be used.

Acknowledgment

The author wishes to thank the Comisión Nacional de la Energía Atómica, Buenos Aires, Argentina, for their support and for permission to publish this paper. Thanks are also due to Gernot Oehley for the wiring of the circuit and the measurements.

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G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y.; 1952.

Correction

The following typographical errors were made in the paper "Conditional-Sum Addition Logic," by J. Sklansky, which appeared on pages 226–231 of the June, 1960, issue of these Transactions.

1) On page 227, in Fig. 1, in the column for $i=11$, for time interval τ_0, where the assumed initial carry is a "1," the carry bit should be a "1".

2) On page 227, in the right-hand column, line 27 should read " . . . *lower* half τ_0-column 1," not " . . . τ_0-column 0."

The author and *Editor* wish to thank E. M. Drogin, Airborne Instruments Laboratory, Deer Park, L. I., N. Y., for calling the above to their attention. Additional errors are:

3) On page 231, (4) should read

$$(p_1 - 1)\, r + 1 \leq p \leq p_1 r.$$

4) On the same page, (6) should read

$$(p_2 - 1)\, r + 1 \leq p_1 \leq p_2 r.$$

Correspondence

A Note on the Simultaneous-Carry-Generation System for High-Speed Adders*

In recent papers[1,2] Weinberger and Smith describe a Simultaneous-Carry-Generation (SCG) system. This is based on the fundamental property of the carry function that the carry C_k from the kth stage of an adder may be treated as a function of the preceding $2k$ addend and augend bits only. The resultant set of nonrecursive logical functions for the sum may be expressed in a large number of alternative ways. Final selection of the nonrecursive or partially nonrecursive form to be used in a circuit realization is a function of available circuit elements, of the properties of units which are to be used and of the speed required from the adder.

The present authors have recently undertaken a detailed study of the various high-speed-carry systems which have been proposed to date.[3,4] An essential feature of all except the Carry-Detection system due to Gilchrist, *et al.*,[5] is that they have to be based on "worst case design." That is, the standard addition time for such arithmetic units is determined by the time required to propagate carry and to add together that combination of operand bits which requires maximum settling time of the addition network. A circuit capable of producing part or all of the sum before expiration of this standard time (excluding any safety margins) is redundant. The SCG system proposed by Weinberger, *et al.*, is redundant in this way since many of the C_k in their circuit are available one or two clock phases before they are required for generation of the sum. Thus it is possible to remove some of the gates in the network without slowing down the system, by delaying the time of appearance of some of the carries.

To illustrate this point we reproduce the equations for the first four carries as quoted in Weinberger and Smith.[2]

	Basic form	Reduced form
$C_1 =$	$A_1 \,\&\, B_1$ $\cup\ (A_1 \cup B_1) \,\&\, C_0$	
$C_2 =$	$A_2 \,\&\, B_2$ $\cup\ (A_2 \cup B_2) \,\&\, C_1$	$A_2 \,\&\, B_2$ $\cup\ (A_2 \cup B_2) \,\&\, A_1 \,\&\, B_1$ $\cup\ (A_2 \cup B_2) \,\&\, (A_1 \cup B_1) \,\&\, C_0$
$C_3 =$	$A_3 \,\&\, B_3$ $\cup\ (A_3 \cup B_3) \,\&\, C_2$	$A_3 \,\&\, B_3$ $\cup\ (A_3 \cup B_3) \,\&\, A_2 \,\&\, B_2$ $\cup\ (A_3 \cup B_3) \,\&\, (A_2 \cup B_2) \,\&\, A_1 \,\&\, B_1$ $\cup\ (A_3 \cup B_3) \,\&\, (A_2 \cup B_2) \,\&\, (A_1 \cup B_1) \,\&\, C_0$
$C_4 =$	$A_4 \,\&\, B_4$ $\cup\ (A_4 \cup B_4) \,\&\, C_3$	$A_4 \,\&\, B_4$ $\cup\ (A_4 \cup B_4) \,\&\, A_3 \,\&\, B_3$ $\cup\ (A_4 \cup B_4) \,\&\, (A_3 \cup B_3) \,\&\, A_2 \,\&\, B_2$ $\cup\ (A_4 \cup B_4) \,\&\, (A_3 \cup B_3) \,\&\, (A_2 \cup B_2) \,\&\, A_1 \,\&\, B_1$ $\cup\ (A_4 \cup B_4) \,\&\, (A_3 \cup B_3) \,\&\, (A_2 \cup B_2) \,\&\, (A_1 \cup B_1) \,\&\, C_0$

The carries are required only for the computing of the final sum during the fifth clock phase. Use of the reduced expressions makes C_2 and C_3 for example available during the second clock phase. By basing their generating circuits on the basic form, these carries become available in the third and fourth clock phase respectively, which is sufficiently early to compute the sum in the final clock phase as required. Thus any extra equipment incorporated to reproduce the reduced equations is redundant. Where standard plug-in units are used this redundancy may not involve waste of equipment but it does increase the amount of back wiring and the number of elements actually in circuit. Hence it decreases reliability and is undesirable.

Similar redundancies occur in the remainder of the carry network. A complete analysis is rather lengthy since these redundancies may be removed in various ways. It would seem that the minimization problem for this circuit taking into account that no carry is *required* before the fifth clock phase, would best be carried through using an automatic computer. It is unlikely however that such a procedure would yield a useful circuit. The authors' current studies have indicated that the SCG system even when improved in the way described and by optimizing the size of gates and the number of phases is less efficient than refined versions of the "Anticipated Carry" (Carry Skip) techniques. It is hoped to describe the latter in the near future.[4]

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* Received by PGEC, April 29, 1960.

[1] A. Weinberger and J. L. Smith, "A one-microsecond adder using one-megacycle circuitry," IRE Trans. on Electronic Computers, vol. EC-5, pp. 65–73; June, 1956.

[2] A. Weinberger and J. L. Smith, "A Logic for High Speed Addition," Natl. Bur. of Standards, Washington, D. C., NBS Circular 591, sec. 1, February, 1958.

[3] N. Burla, "Some Logical Problems in the Design of a High Speed Adder for Parallel Binary Digital Computers," thesis presented in partial fulfillment of the requirements for the M.Sc. degree at the Technion, Israel Inst. of Tech., Haifa, May, 1960.

[4] M. Lehman and N. Burla, "Skip techniques for high speed carry propagation in binary arithmetic units," to be published.

[5] B. Gilchrist, J. H. Pomerene, and S. Y. Wong, "Fast carry logic for digital computers," IRE Trans. on Electronic Computers, vol. EC-4, pp. 133–136; December, 1955.

Periodic Binary Time Series and Their Relation to Boolean Functions*

In a previous note,[1] the author show how any binary time series $f(t)$ of length can be written as a sum of periodic functio with periods respectively of 1, 2, 4, · · 2^p. These periodic functions are given as

$$f_k(t) = \frac{(t+k)!}{t!k!},$$

taken modulo two, or as $g_k(t)$, where $g_k(t)$ the time reverse of the functions $f_k(t)$. F instance, $g_0(t) = 1111 \cdots$; $g_1(t) = 0101 \cdots$ $g_2(t) = 00110011 \cdots$ etc. (See van Heerde for a simple way of generating these fur tions.) By writing the number t in bina digits, $t = x_p x_{p-1} \cdots x_3 x_2 x_1$, $f(t)$ can looked upon as a Boolean function of p va ables $f(t) \rightarrow f(x_p, x_{p-1}, \cdots, x_3, x_2, x_1)$. Th is worthwhile to consider, since especia the $g_k(t) \rightarrow g_k(x_p, x_{p-1}, \cdots x_3, x_2, x_1)$ assur a particular simple form as such. It com out that

$$g_0(x) = 1, \quad g_1(x) = x_1, \quad g_2(x) = x_2$$
$$g_3(x) = x_2x_1, \quad g_4(x) = x_3, \quad g_5(x) = x_3$$
$$g_6(x) = x_3x_2, \quad g_7(x) = x_3x_2x_1, \quad g_8(x) = x_4$$
etc.

The rule is that if n functions are give where $n = 2^p$, the next higher n functions a obtained by multiplying the first n functio with x_{p+1}. This rule can be stated in a st simpler form for any g_k: Write k as a bina number

$$k = x_p{}^0 x_{p-1}{}^0 \cdots x_3{}^0 x_2{}^0 x_1{}^0;$$

then g_k is given as the continuous produ $\prod_i x_i$, such that x_l occurs in this product $x_l = 1$, and x_l does not occur if $x_l{}^0 = 0$, or formula:

$$g_k(x) = \prod_1^p [1 + x_i{}^0(1 + x_i)].$$

As an application, it follows that t same simple computation used for the B [the coefficient of the g_k's if $f(t)$ is giv can also be used for writing in general Boolean function in p variables as a modu two sum of these simple Boolean functio provided its value in each point is know

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* Received by the PGEC, August 8, 1960.

[1] P. J. van Heerden, "Analysis of binary time ries in periodic functions," IRE Trans. on El tronic Computers, vol. EC-8, pp. 228–229; Ju 1959.

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Upon graduation, he joined the Product Development Laboratory of the IBM Corporation at Poughkeepsie, N. Y. His initial assignment was in the area of machine design and circuit packaging for STRETCH. Since then he has worked the design of switching circuits. He is sently in charge of a group designing h-speed circuits.

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William Comley was born on September 14, 1921, in Indianapolis, Ind. After completing the electronics curriculum at Los Angeles City College, he served as a communications officer with the U. S. Air Force for three years, and was responsible for the operation of high-powered radio teletype facilities. He subsequently augmented his education with undergraduate and graduate studies at the University of California at Los Angeles, and the California Institute of Technology, Pasadena.

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In 1947, he joined the engineering staff of Lear, Inc., Santa Monica, Calif., as a design engineer in aircraft radio. He later, served as project engineer for that company's line of phonograph pickups and magnetic recording heads. He joined the Douglas Aircraft Company, Inc., El Segundo, Calif., in 1950. A computer specialist, he is engaged in the design of special analog devices and data reduction systems.

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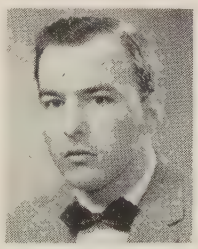

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He was associated with Magnetics Inc., Butler, Pa., from 1952 through 1953, where he worked on the development of magnetic amplifier circuits. He was an assistant professor at Carnegie Institute of Technology from 1956 to 1958 and joined the Magnetic Logic Circuits Group of IBM Research in 1956. At present he is with the Advanced Systems Development Division of IBM where he has been working on exploratory devices and circuits.

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Arthur Gill, for a photograph and biography, please see page 126 of the March, 1960, issue of these Transactions.

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He joined the Burroughs Corporation Research Center in 1952 and was engaged in solid-state digital computer circuit design. In addition, he is experienced in logical design for digital computers, power supply design, servo system design, and magnetic circuit design. Since early in 1958, he has been concerned with the development of new computer circuit techniques, with special emphasis on high-speed nondestructive memories. He was group leader on the recently developed Fluxlok Memory technique. He is presently supervisor of the magnetics circuits design section.

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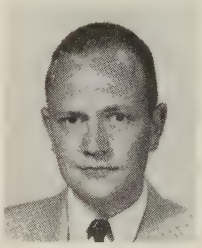

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During the academic year 1954–1955, he held a Pre-Doctoral Fellowship from the National Science Foundation and conducted research on psychoacoustic problems at the Electronic Defense Group of the University of Michigan. In 1956–1957 he again held a National Science Fellowship and spent the year at the Massachusetts Institute of Technology, Cambridge, as a Visiting Fellow of the Economics and Social Sciences Department, where he worked on problems concerned with auditory detection. Since 1958 he has been assistant professor at M.I.T., teaching courses in general psychology, and consultant at Bolt, Beranek and Newman, Inc.

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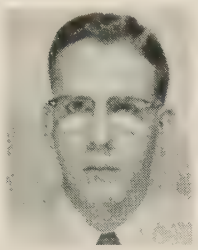

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From 1953 to 1957, he was employed by Hughes Aircraft Company, Culver City, Calif., where he was engaged in the development of transistor circuitry for airborne digital computers. In 1957 he joined the General Electric Computer Laboratory, Palo Alto Calif., where he developed transistor circuits for magnetic core and magnetic drum memories. In 1958 he became a research assistant at Stanford University. He is presently an associate professor of electrical engineering at the University of Arizona, Tucson, and is conducting research in solid-state electronics.

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Joseph J. Karew (M'56) was born in Worcester, Mass., on March 30, 1924. He received the B.S. degree in electrical engineering from the Illinois Institute of Technology, Chicago, in 1952.

He then became a member of the Philco Corporation's Research Division, Philadelphia, Pa., assigned to the semiconductors circuit application group. In 1956, he joined the Burroughs Corporation Research Center, Paoli, Pa., where he has worked extensively on advanced solid-state circuit design. Two patent applications have been filed in connection with his work at Burroughs for a crystal-controlled blocking oscillator and for a trailing edge trigger technique for bistable multivibrators. Since 1959 he has headed the digital circuits section in the Electronics Department.

J. J. KAREW

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Ladis D. Kovach (A'53–M'58) was born on November 21, 1914, in Budapest, Hungary. He received the B.S. degree in physics in 1936 and the M.S. degree in mathematics in 1948 from Case Institute of Technology, Cleveland, Ohio; the M.A. degree in education from Western Reserve University, Cleveland, in 1940; and the Ph.D. degree in mathematics from Purdue University, Lafayette, Ind., in 1951.

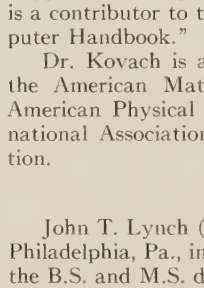
L. D. KOVACH

From 1936 to 1948, he was associated with Picker X-Ray Corporation, American Shipbuilding Company, and Ohio Crankshaft Company, Cleveland, as electrical designer. Since 1951, he has been with the Douglas Aircraft Company, Inc., El Segundo, Calif., where he is a design specialist in charge of the analog computer facility. Since 1958, he has also been professor of mathematics and acting head of the Department of Mathematics and Physics at Pepperdine College, Los Angeles, Calif. He is a contributor to the McGraw-Hill "Computer Handbook."

Dr. Kovach is a member of Sigma Xi, the American Mathematical Society, the American Physical Society, and the International Association for Analog Computation.

❖

John T. Lynch (S'55–M'56) was born in Philadelphia, Pa., in 1927. He received both the B.S. and M.S. degrees in electrical engineering from Pennsylvania State University, University Park, in 1954 and 1955, respectively.



J. T. LYNCH

He is currently manager of the Electronics Department of the Burroughs Research Center in Paoli, Pa. Since joining Burroughs in 1955, he has performed circuit configuration analyses for mi tary and commercial applications, and h designed numerous transistorized logical ci cuits. In his present assignment he is respo sible for circuit design and system tests computers under development for a varie of military applications.

Mr. Lynch is a member of RESA.

❖

Thomas Marill was born in Berlin, Ge many, on February 13, 1929. He receive the B.A. degree from Swarthmore Colleg Pa. in 1951, the M.. degree from Corn University, Ithac N. Y. in 1953, ar the Ph.D. degr in psychology fro Massachusetts Inst tute of Technolog Cambridge, in 195

T. MARILL

In the period fro 1952 to 1958, h was connected wit M.I.T., serving c the staffs of th Acoustics Laboratory, the Research Lab oratory of Electronics, and the Lincoln Lab oratory. He was engaged in studies of math matical models of sensory processes, dete tion theory, display problems, psychoacou tics, human engineering, and computer tech niques. Since 1958, he has been a senior co sultant at Bolt, Beranek and Newman In where he has been concerned with syste studies, computer applications, and artifici intelligence.

Dr. Marill is a member of the America Psychological Association, the Psych metrics Society, and the ACM.

❖

Robert J. Martin was born on July 2 1926, in Detroit, Mich. He received th B.S.E.E. degree from the University c Michigan, Ann Ar bor, in 1951. Afte being recalled int the U. S. Navy, h returned to the Uni versity of Michigan He received the M.S degree in 1954, and i currently working i the Electron Physic Laboratory and con tinuing his studie towards the Ph.D degree in electrica engineering. His primary interest is in th field of gaseous conduction.

R. J. MARTIN

Mr. Martin is a member of Sigma Xi an Phi Kappa Phi.

❖

Nino A. Masnari was born on Septembe 20, 1935, in Three Rivers, Mich. He receive the B.S. and M.S. degrees in electrical engi neering in 1958 and 1959, respectively, fro the University of Michigan, Ann Arbo where he is now a doctoral candidate.

Since 1957, he has been associated with e Electron Physics Laboratory of the niversity of Michigan Research Institute and is presently a research assistant. During the past two years he has been working with an analog computer as an aid in the investigation of electron motion in various types of microwave tubes. He has been primarily concerned with the design of crossed-field tubes and the fect of space-charge in such devices.

N. A. Masnari

Mr. Masnari is a member of Eta Kappa u and Tau Beta Pi, and an associate mem-er of Sigma Xi.

❖

Jan A. Narud (S'51-A'52-M'57) was born Oslo, Norway, on June 3, 1925. He re-eived the B.S. and M.S. degrees from the California Institute of Technology, Pasadena, in 1951, and the Ph.D. degree from Stanford University, Stanford, Calif., in 1955.

J. A. Narud

He then joined the staff of Harvard University, Cambridge, Mass., as an assistant professor in the Division of Engineering and Applied hysics until 1960. Here he taught courses automatic control, transistor circuits and nformation theory, and directed the re-earch activities in the fields of active net-orks and control systems. During 1957–959, he was also a consultant to Bell Tele-hone Laboratories, where he worked on arious problems in pulse code modulation. n 1959, he joined the Mohansic Research aboratory of the IBM Corporation in Yorktown Heights, N. Y.

Dr. Narud is a member of Sigma Xi.

❖

Gordon W. Neff was born in Genesee, . Y. on June 20, 1934. He received the .S.E.E. degree from Syracuse University, Syracuse, N. Y., in 1956, and did graduate work at Brown University, Providence, R. I., in applied mathematics in 1958. In August, 1960, he returned to Brown under the IBM Fellowship Program to complete his graduate studies.

G. W. Neff

In 1957, he joined the Product Develop-ent Laboratory of IBM in Poughkeepsie, . Y., doing developmental work on high-peed transistor switching circuits. In June, 958, he went to the Research Division of BM, working on device application. When the Advanced Systems Division of IBM was originated in 1959, he was assigned to a group in this division responsible for non-mechanical memory development.

Mr. Neff is a member of Eta Kappa Nu, Pi Mu Epsilon and Tau Beta Pi.

❖

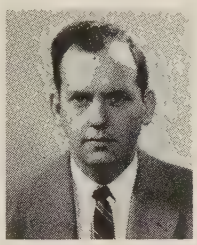
Nedeljko Parenzanović was born on August 25, 1932, at Ivanjica, Yugoslavia. He graduated from the Faculty of Natural Sciences of the University of Belgrade in 1957.

N. Parezanović

He is now employed in the "Boris Kidrich" Institute of Nuclear Sciences in Belgrade and is working on the repetitive differential analyzer in the Department of Numerical Analysis.

❖

Joseph E. Rowe was born on June 4, 1927, in Highland Park, Mich. He received the B.S. degree in electrical engineering and mathematics in 1951, the M.S. degree and the Ph.D. degree in electrical engineering in 1952 and 1955, respectively, from the University of Michigan, Ann Arbor.



J. E. Rowe

Since 1951 he has been associated with the University of Michigan Research Institute, engaged in fundamental research on microwave systems, microwave devices, and electromagnetic field theory. Formerly a lecturer, assistant professor of electrical engineering, and associate professor of electrical engineering, he is now professor of electrical engineering and director of the Electron Physics Laboratory at the University of Michigan.

Dr. Rowe is a member of the American Institute of Electrical Engineers, the American Mathematical Society, and the Society for Industrial and Applied Mathematics. He is also a member of Sigma Xi, Phi Kappa Phi, Tau Beta Pi, and Eta Kappa Nu.

❖

Forrest O. Salter was born in Charlottesville, Va., on February 26, 1927. He received the B.S. degree in electrical engineering from Milwaukee School of Engineering, Wis., in 1950.

F. O. Salter

From 1950 until 1957, he worked for SimpsonElectric Company, Chicago, Ill., in design of electronic instruments. Since then he has been at Argonne National Laboratory, Argonne, Ill., in the computer section of the Applied Mathematics Division, where he has been doing circuit design work for a transistorized computer.

❖

Mauricio A. Thomae (S'53–A'54) was born in Buenos Aires, Argentina, on July 20, 1928. He received the degree of Telecommunication Engineer from the Buenos Aires University in 1954.

M. A. Thomae

In 1951 he joined the Comisión Nacional de la Energía Atómica, Electronic Department, as a laboratory assistant, working in nuclear instrumentation. From 1955 to 1956, he was with Siemens Argentina, as a factory engineer, spending five months in Munich, Germany, in a Siemens & Halske tubes factory, studying electrical tests in tube production. In 1956, he returned to the Comisión Nacional de la Energía Atómica, and has since been working in nuclear instrumentation applied to measurements and control of physical variables related to that field.

Mr. Thomae is a member of the Asociación Argentina de Electrotécnicos in Buenos Aires.

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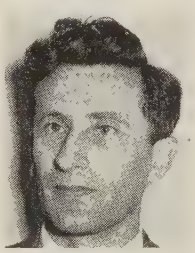
Rajko Tomović was born in Baja, Hungary, on November 1, 1919. He received the B.S. degree in electrical engineering from the University of Belgrade, Yugoslavia, in 1946.



R. Tomović

After graduation, he joined the Power Engineering Institute in Belgrade, where he was engaged in designing computers for the study of electrical transmission systems. In 1950, he spent the summer at the Massachusetts Institute of Technology, Cambridge, as the Yugoslav participant of the Foreign Student Summer Project, and in 1952, received the Doctor's degree from the University of Belgrade for research work in analog computers. In 1951, he joined the "Boris Kidrich" Institute of Nuclear Sciences in Belgrade, as research associate of the Laboratory of Applied Mathematics. He is now the head of the new Laboratory of Automatic Control.

Dr. Tomović is Vice President of the International Association for Analog Computation.

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Gilbert C. Vandling (S'56-M'58) was born on July 19, 1932, in Danville, Pa. He was an aviation electronics technician and instructor in the U.S. Navy from 1951 to 1955. He received the B.S.E.E. degree from Illinois Institute of Technology, Chicago,

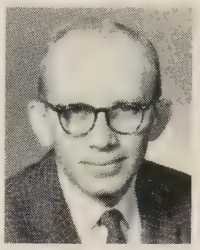
in 1958 and the M.S.E.E. degree from Syracuse University, Syracuse, N. Y., in 1960.

G. C. Vandling

In 1958 he joined the General Electric Company as a member of the Honors Program for graduate study. He joined the information Processing Component of the General Electric Electronics Laboratory, Syracuse, N. Y., in 1959, where he has been engaged in switching theory research and logical design.

Mr. Vandling is a member of Tau Beta Pi and Eta Kappa Nu.

Gerard P. Weeg (M'57) was born on October 29, 1927, in Davenport, Iowa. He received the B.S. degree in mathematics from St. Ambrose College, Davenport, in 1949, and the M.S. degree in mathematics from Oklahoma State University, Stillwater, in 1950. In 1955 he received the Ph.D. degree in mathematics from Iowa State University, Iowa City.



G. P. Weeg

He held the position of instructor in mathematics at St. Ambrose from 1950 to 1952. From 1954 to 1956, he was a mathematician in desig guidance at Remington Rand Univac Divi sion of Sperry Rand in St. Paul, Minn. I 1956 he was made an assistant professor i mathematics at Michigan State University East Lansing. He then took a joint appoint ment between the Department of Mathe matics, Electrical Engineering, and the Com puter Laboratory at that University in 1957 He was made an associate professor in 1959

Dr. Weeg's field of interest has bee computer-oriented mathematics, with publi cations appearing in the areas of numerica analysis, switching circuit theory, and finit automata.

He is a member of the American Mathe matical Society, the Mathematical Asso ciation of America, and the ACM.

Reviews of Books and Papers in the Computer Field

E. J. McCluskey, Jr., review editor
W. J. Cadden, asst. review editor
T. C. Bartee, asst. review editor

Please address your comments and suggestions to the Reviews Editor, Prof. E. J. McCluskey, Jr., Dept. of Elec. Engrg., Princeton University, Princeton, N. J.

Combinational Switching Circuit Theory and Boolean Algebra

Functional Canonical Form—H. Allen Curtis. (*J. Assoc. Comp. ach.*, vol. 6, pp. 245–258; April, 1959.)

Considerable effort in the field of combinational switching theory s been devoted to the determination of techniques for optimum sign. Unfortunately, the elusive nature of a general concept of op- num has resulted in methods which are a combination of a deter- nistic procedure and an experimental art. This is the main disad- ntage of this paper: that it is just another approach, among many, this difficult problem. While this may be of interest to the collector "optimum" techniques it offers no deeper insight into the more neral problem.

As stated by the author, an approach which relies on the structural operties of the switching functions representing the final network uld probably have a greater chance of achieving a satisfactory lution. The actual approach adapted here, however, is simply an trapolation of the role of the tree circuit in the optimum design of ay circuits. This extrapolation is obtained by first noting that the nonical form corresponding to a tree circuit can be obtained by nsidering recursively the switching function and its associated bfunctions in the form

$$x_1, x_2, \cdots, x_n) = x_n \cdot \phi(x_1, x_2, \cdots, x_{n-1}) + x_n' \cdot \theta(x_1, x_2, \cdots, x_{n-1}).$$

his, the author notes, is a breakdown where the basic building ocks are functions of three variables,

$$f(x_1, x_2, \cdots, x_n) = F(\phi, \theta, x_n),$$

d perhaps a breakdown where the basic building blocks are func- ons of two variables might be more effective. One form, for example,

$$f(x_1, x_2, \cdots, x_n) = x_n \cdot (\phi \Delta \theta) \Delta \theta$$

here Δ is the "exclusive or." Other more general formulations are ven in the paper, but the use of the "exclusive or" appears in some ses unavoidable.

While such an approach is of theoretical interest, the technique pears to be of limited usefulness. In particular, the operation xclusive or" usually costs more than "and" or "inclusive or" except a few specialized circuits. Examples using this technique to mini- ze the number of control grids of vacuum tube circuitry are given. o other physical configurations are considered. Another important ission is the applicability of the technique when "don't care" nditions are present.

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plied Boolean Algebra, an Elementary Introduction—book by anz E. Hohn. (The Macmillan Co., New York, N. Y.; 1960. 139 ges+xx pages, Illus. 6×9. $2.50. Paperback.)

This little book presents the basic facts of Boolean algebra and de- ibes some of its applications—in particular, applications to switch- g circuits. The treatment is intended for both mathematicians and gineers. No special engineering or mathematical background is as- ned; however, a certain maturity is correctly assumed to be a necessary requirement for profitable reading of this work. This little volume, which is printed by a photo-offset process, contains material which is to become part of a more substantial work on Boolean algebra and its applications. The purpose of this preliminary version is two-fold: "to make the way easier for those who need to learn Boolean algebra because of its applications to computer and switching design," and "to invite other readers, whose interests may be casual, to study more seriously this interesting and increasingly important subject." In the opinion of this reviewer, the book is highly successful on both counts.

In the Introduction, a Boolean algebra is abstractly defined and a number of useful theorems are derived, in order to emphasize that this algebra is a mathematical structure independent of its applications. However, in the remainder of the book, the emphasis is on Boolean algebra as applied mathematics rather than as abstract algebra. The next three chapters, respectively, present an intuitive introduction to Boolean algebra as a model of a class of simple switching circuits, show that the same algebra provides a theory of propositional functions, and interpret the same algebra as the algebra of subsets of a set. A fourth chapter discusses the minimization problem within the framework of the Veitch-Karnaugh map method. Two appendixes deal briefly with the binary system of numeration and semiconductor logic elements.

Although the approach taken in the book is intuitive and the subject matter is developed in an elementary way, the treatment achieves a certain depth not always reached in existent textbooks dealing with the application of Boolean algebra to switching circuits. The first chapter, which treats Boolean algebra as a model of combinational relay circuitry, although well done, might be classified as a standard treatment of the subject, as presented in current textbooks. However, the second and third chapters which deal with the same algebra as a model of propositional logic and of the subsets of a set, respectively, present concise and extremely clear treatments of material which is usually not so well treated in elementary texts. The integrated treatment of these several aspects of Boolean algebra provides the beginner with valuable understanding and perspective on the whole subject. The material of the book is very well organized and, for a preliminary edition, is remarkably free of errors. The style and clarity of expression reveal the hand of a fine mathematician who has also considerable literary ability. The exercises (70 in number) are well chosen to bring out the main points of the material and, in many cases, to develop part of the theory. The references appear to have been carefully selected, are relevant to the material presented, and are adequate for the intended purpose.

There is a temptation to criticize the book for what it does not contain. For example, the treatment of the minimization problem is brief, and the presentation involving only the Veitch-Karnaugh method seems too restrictive. The discussion of semiconductor logic in the second appendix would not satisfy the engineer,but might be adequate for the mathematician with no previous knowledge of the subject. However, the author clearly states his position, namely, that none of the chapters pretends to be complete and that each goes just far enough to establish the connection between the application in question and the basic rules of Boolean algebra. Under these ground rules, the author clearly achieves his goal.

This small volume, which might well serve as a primer for future textbook writers, has whetted our appetites for the subject; we anxiously await the main course to come.

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Algebraic Topological Methods in Synthesis—J. Paul Roth. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University Press, Cambridge, Mass., vol. 29, pp. 57–73; 1959.)

This paper forms part of a series of generally quite excellent papers presented at the Harvard International Symposium on Switching Theory in 1957, and gives the author's solution to what in the early days of switching theory was known as "Quine's problem," or the problem of finding irredundant normal forms of truth functions (shortest "sums of products" and "products of sums"). Viewed from an algebraic topological standpoint, the problem becomes one of finding for a given cubical complex K of an n-cube a K-cover of minimum cost. Two algorithms for the solution of this covering problem are offered in the paper: one that requires a complete listing of all the maximal cubes, or cocyles of K (in logical notation: prime implicants), and one that does not. Both algorithms are general in that K may contain a subcomplex L where the vertices of K-L are so-called "don't care" vertices. The problem then is to find a K-cover of L of minimum cost.

The basic steps of the first, or "extraction" algorithm are:

1) Determination of Z, the space of all cocyles of K.
2) Determination and removal of E_1, the space of all L-extremals of K. (The latter are cocycles of K which contain a vertex of L not contained in any other cocycle of K.)
3) Introduction of an iterative procedure for finding and removing from the remaining cocycles of Z all second-order extremals (L-extremals of the complex L_2 generated by the vertices of L *not* in E_1), third-order extemals (L-extremals of the complex L_3 generated by the vertices of L_2 *not* in E_2), and so on, until all vertices of L have been covered by an L-extremal. A minimum K-cover of L then is simply $E_1 \cup E_2 \cup \ldots$ (In the event that complex L_i has no extremals, a branching operation is introduced whereby a cocycle z_i is treated, first as if it *were* an extremal of L_i and then as if it were *not*, in order to obtain minimum covers.)

The second, or "local-extraction" algorithm differs from the first in that it does not require determination of *all* cocycles of K and, at any stage of the reduction, only one extremal at a time must be found, and this by means of a local computation only. Although the reviewer finds the second algorithm extremely interesting in its own right, he feels he cannot adequately do justice to them both within the confines of a review. Consequently, his remarks will be directed toward the "extraction" algorithm only.

On a subject like minimization, about which much has been written, it is natural to try to compare and evaluate the approaches taken by different authors and their methods of solution. However, only a brief start toward such a large undertaking can be made here. Consider first the approaches. If, as C. S. Peirce contends, a good language is the essence of good thought, then it is important to pay attention to the kind of language that is used to formulate the normal form problem. What should be the criteria for a good language for thinking about the problem? I think everyone would agree that the language should possess a strong intuitive power capable of yielding a mechanization and visualization of the problem that would not be evident to the same degree were another language used. In brief, the language should lend itself readily to the discovery of some inherent structure of the problem from which can be fashioned the essentials of a solution. Thus the more readily discernible the structure of the problem and the interrelations of its parts, the better suited is the language to solve the problem.

In the reviewer's opinion the logical approach yields a visualization of the requirements of the normal form problem not evident from the standpoint of algebraic topology. In his first paper[1] on the subject in 1952, Quine struck at the heart of the covering problem when he observed that the test for determining whether a cover is irredundant is to see whether any of its prime implicants *imply* the disjunction of remaining prime implicants. The significance of this fact, however, was not fully appreciated until Gazale showed a way to compute these implication relations by the method of ratio functions.[2] The reviewer's own method of iterated consensus of the prime implicants,[3] which provides an alternate way of determini these important branching conditions, owes its existence to Gazal acumen on this point.

So much for approaches. In order to compare the "extractio algorithm with alternate procedures, it is necessary to establish so sort of common denominator. Restated in terms of logical notatic the basic steps of the "extraction" algorithm are:

1) determination of all the prime implicants,
2) determination and removal of all core clauses,
3) selection from the remaining prime implicants of a subset prime implicants which together with the core comprises irredundant covering.

The way in which the steps of the "extraction" algorithm a actually carried out is seen to have its counterpart in the table prime implicants. Thus step 2, the removal of all L-extremals of corresponds to the deletion of these clauses from the row of prir implicants which cover a canonical term (min-term) not covered any other prime implicant. Then if every canonical term covered by core prime implicant is removed from the column of min-terms, st 3 becomes the iterative procedure of deleting from the remaini rows those prime implicants which, again, cover a remaining canonic term not covered by any other prime implicant, and so on, until min-terms have been so removed. The disjunction of prime imp cants thus deleted comprises an irredundant covering of the mi terms. In the event that a stage of the reduction is reached whe none of the remaining canonical terms are covered by exactly one the remaining prime implicants, a branching operation is introduc whereby a given prime implicant is a) assumed to be in a minimu covering and then removed along with the min-terms it covers a the reduction operation continued, and b) assumed to be in no mir mum cover, and removed while the canonical terms covered by it a left intact and the reduction process continued.

The method of detecting L-extremals of K is thus seen to be ide tical to the method advocated by Quine,[1] Petrick,[4] and M Cluskey[5] for finding core prime implicants. It should be noted th other procedures[2,3] exist in the literature for locating cor based on the property that none of the core prime implicants imp a disjunction of remaining prime implicants.

It is difficult to compare step 3 of the "extraction" algorith the branching procedure, with similar procedures employed in t methods cited in the previous paragraph. Suffice it to say that have ways of accomplishing branching that appear to be sufficient systematic for use with a digital computer.

Although both are topological in character, there would appe to be little that is common between the "extraction" algorithm ar the Urbano-Mueller algorithm.[6] The basic idea behind the latt algorithm is that the determination of an irredundant cover of given cubical complex K of an n-cube is made to depend upon the d termination of an irredundant cover of some smaller complex ge erated by a subset of the vertices of K. This is accomplished by fin ing for every vertex v_i of K the set of cocycles that cover v_i (called t basic star of v_i) and removing from consideration all vertices K whose basic stars contain other basic stars as proper subsets.

One final remark. It remains true that the proof of any puddin no matter how artfully it is conceived, lies in its eating. The "extra tion" and sister algorithms have proved their workability beyond a shadow of a doubt; the same *remains* to be said of others. Perhaps the final analysis it is only by measuring the degree of success achieve by its computer program that one should attempt to judge the mer of an algorithm.

Several minor typographical errors were noted, especially pages 62, 63. On page 66, line 11 from the bottom, "cost $u \leq$ cost should read "cost $u \geq$ cost v."

T. H. Mott, J
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Princeton, N.

[1] W. V. Quine, "The problem of simplifying truth functions," *Am. Math. Monthly*, vol. 59, pp. 521–531; October, 1952.
[2] M. J. Gazale, "Irredundant disjunctive and conjunctive forms of a Boolean function," *IBM J. Res. & Dev.*, vol. 1, pp. 171–176; April, 1957.
[3] T. H. Mott, "Determination of the irredundant normal forms of a truth fun tion by iterated consensus of the prime implicants," IRE TRANS. ON ELECTRON COMPUTERS, vol. EC-9, pp. 245–252; June, 1960.
[4] S. R. Petrick, "A Direct Determination of the Irredundant Normal Forms o Boolean Function from the Set of Prime Implicants," AF Cambridge R Center, Bedford, Mass., TR-56-110; April, 1956.
[5] E. J. McCluskey, "Minimization of Boolean functions," *Bell Sys. Tech. J.*, v 35, pp. 1417–1444; November, 1956.
[6] R. H. Urbano and R. K. Mueller, "A topological method for the determinati of the minimal forms of a Boolean function," IRE TRANS. ON ELECTRONIC CO PUTERS, vol. EC-5, pp. 126–131; September, 1956.

coding of Incompletely Specified Boolean Matrices—T. A. Dolotta H E. J. McCluskey, Jr. (*Proc. WJCC*, pp. 231–238; May 3–5, 1960).

The authors consider a synthesis problem exemplified by the de- n of a control element for a digital machine. The control element nsidered is to consist of a combinational logical network with p tput lines and n input lines. The p output lines are to provide the ntrol signals for the machine, and the n input lines are to contain operation code for a given one of m different instructions (where $\leq 2^n$). The paper considers a systematic procedure for assigning operation code representation to each of the m instructions, with iew toward minimizing the combinational network.

The p output functions are written in the form of an $m \times p$ matrix, ere each matrix element is a 0, a 1, or a ϕ, the latter symbol desig- ting "indifferent" outputs. Specific rules are provided for simplify- the matrix, basically resulting in the reduction of the number of lumns in the matrix. The assignment of n-bit numbers to the m ws of the simplified matrix follows. In general the procedure appears ry efficient, and in some cases it results in a network which can be own to be minimal. Examples are also given; the major example is ken from a previous paper on this subject and results are compared. is example does not exploit the technique fully, and a further ample would have been of interest. The principal advantage of the thods presented is their systematic nature which lends itself to plementation by computer programs.

The material is very well presented, and considerable care has en taken in the preparation of the paper. The reviewers suggest at the paper might well serve as a guide for other authors in a ld not noted for clarity.

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achine Analysis of Switching Circuits—P. P. Parkhomenko. *utomation and Remote Control*, vol. 20, April, 1959; English trans- ion published January, 1960.)

e Analysis and Synthesis of Certain Discrete Contactless Circuits— I. Rameev and Yu. A. Shreider. (*Automation and Remote Control*, l. 20, January, 1959; English translation published July, 1959.)

inimization to the Boolean Functions Characterizing Switching rcuits—M. A. Gavrilov. (*Automation and Remote Control*, vol. 20, ptember, 1959; English translation published January, 1960.)

The three papers reviewed here appeared in the English language rsion of the Soviet journal, *Avtomatika i Telemekhanika*, which published by the Instrument Society of America with the aid a grant from the National Science Foundation. The number of ferences to American authors in the bibliographies of these papers dicates the familiarity of Soviet authors with American works; the latively few references to Soviet papers in the bibliographies of our urnals may indicate some lack of communication in our direction. eadily obtainable translations of Soviet journals such as this monthly ould help alleviate this situation.

The first paper, "Machine Analysis of Switching Circuits," is de- ted primarily to a description of the Soviet IAT AN SSR, a spe- l-purpose digital machine which has been constructed to analyze tomatically the operation of relay circuits. The first section of the per presents a brief discussion of several prior machines of this type, cluding the familiar (to American readers) Shannon and Moore ay-circuit analyzer,[1] as well as the Soviet machines of Tsukanov d Rodin.

The IAT AN SSR is then described. This machine has the capac- of analyzing relay circuits of up to twenty elements. (A description an earlier model may be found in Gavrilov.[2]) Physical models of e circuits to be analyzed are used, being implemented by means of a ug-board and the necessary components. Outputs from the ma- ine are from either lights or a printer. Parkhomenko describes the sic philosophy of the machine in some detail, including the algo- hm which is used to determine the structure of sequential circuits. Several block diagrams and photographs illustrating the integral parts of the machine are included.

The last section of the paper sets forth some possible future applications, including the analysis of circuits composed of solid-state elements (by constructing an equivalent relay circuit), comparison of relay circuits, evaluation of logical expressions, and automatic quality control. Parkhomenko also looks forward to the synthesis of switching circuits using general-purpose computers; this reviewer is in accord.

It is interesting to note that the IAT AN SSR was chosen for a Grand Prize at the 1958 Brussels exposition.

The second paper, "The Analysis and Synthesis of Certain Discrete Contactless Circuits," discusses the design of diode switching circuits for the Strela computer, although the circuits and techniques described are quite general and conventional. The synthesis and analysis is based on a "variant of the ordinary Boolean algebra, and not less simple than this latter."

This paper actually provides an introduction to conventional AND and OR gate diode circuits, and a description of some basic techniques for the analysis and synthesis of combinational circuits using the propositional calculus. The explanation of the use of the formulas of the propositional calculus to analyze switching circuits, the illustrations of the physical realization of the operations on variables, the assignments of the symbols 0 and 1 to the two values of potential used as signals, and the derivation of a system of formulas describing a circuit, etc., will appear familiar to a follower of current switching theory literature, but the basic ideas are developed clearly, with maturity in the presentation and a reasonable amount of rigor.

In the later sections the authors present a systematic technique for deriving a formula of the propositional calculus which describes or corresponds to a given physical network, and for converting this formula to what is generally referred to as *canonical* or *expanded normal form*. Following this there are some remarks on simplification, each of which is motivated by means of a specific circuit. Again, the presentation is at an introductory level. One point may be noted: Fig. 9 shows a simplified version of the circuit in Fig. 8, but Fig. 9 may also be simplified, with a saving of 4 diodes and a corresponding reduction of two levels in circuit complexity.

The article ends with the design of a full adder using only diode logic: first, two single-output circuits are designed, one for the sum output and one for the carry output; this is followed by a three-level, multiple-output, full adder. In all, this paper presents nothing new but is an excellent introductory article to diode logic.

The third paper, "Minimization of the Boolean Functions Characterizing Switching Circuits," is by M. A. Gavrilov, a leading name in Soviet switching literature. This paper may be divided into two sections; the first deals with the minimization of single Boolean expressions in normal (disjunctive) form, and the second with the synthesis of a class of sequential circuits. The bibliography of this paper shows that the author is conversant with American switching literature; 10 of the 18 references are to American authors.

The minimization technique proceeds, as does the Quine technique which is referenced, in two steps: first, a set of minimal terms is derived from the expressions to be minimized, and second, a subset of these terms is selected. "Forbidden input states" and "indifferent output states" ("don't cares") are nicely handled in both the written description and symbology. Gavrilov's approach is straightforward: least number of literals is the criterion for minimality; the first theorem asserts that the minimal expression must consist of minimal product terms (prime implicants, in effect); the first procedure for deriving these terms consists of generating all product terms in the input variables, starting with single variables and adjoining variables and their complements while testing each new term to see if it "realizes" an input state which should cause a 0 output. The shortest terms which do not realize forbidden inputs are the minimal terms. All of this is nicely developed and explained; some is an extension of previous work by Gavrilov.

The selection of terms for the minimal expression(s) is effected using the technique described by Petrick[3] and McCluskey,[4] which consists of forming a product-of-sums expression describing the prime implicant table for the problem and converting this to sum-of-products form. For some reason, the set of necessary terms,

[1] C. E. Shannon and E. F. Moore, "Machine aid for switching circuit design," oc. IRE, vol. 41, pp. 1348–1351; October, 1953.
[2] M. A. Gavrilov, "A survey of research in the theory of relay networks in the SR," *Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The nals of the Computation Laboratory," Harvard University Press, Cambridge, ss., vol. 29, pp. 26–53; 1959.

[3] S. R. Petrick, "A Direct Determination of the Irredundant Forms of a Boolean Function from the Set of Prime Implicants," AF Cambridge Res. Center, Bedford, Mass., Tech. Rept. No. 56–110; April, 1956.
[4] E. J. McCluskey, "Minimization of Boolean functions," *Bell. Sys. Tech. J.*, vol. 35, pp. 1417–1444; November, 1956.

or core, is not removed first. In both of the sample problems illustrated, removal of the core will obviate the need for the more complicated symbolic procedure.

The second theorem and its use in the minimization procedure is new, at least to the reviewer, and of interest. The theorem asserts that "a Boolean function expressed with normal form F', which has one or several terms of length less than minimal, that is, terms which realize not only all the f_i, but also certain f_0, can be taken to a normal form which realizes only f_i if, for the conditions f_0 mentioned above, one sets up one of the partial minimal forms Ψ and then takes the product $F'\Psi$." (The f_i are product terms corresponding to inputs which shall yield l outputs, and the f_0 should yield 0's.) The paper then shows how under certain constraints, which are quite severe, the product $F'\Psi$ will be a minimal form (an irredundant normal form). As Gavrilov states, this algorithm will not generally be useful in deriving minimal forms, but it may be used to speed up the process of shortening the forms. (It could them be followed by some other procedure such as consensus taking.[5])

The remainder of the paper presents a procedure for the conversion of a table containing the statement of a sequential circuit problem, to a set of minimal expressions, each expression describing a particular output line. This section of the paper contains references to previous works of Gavrilov and other Soviet authors, which may not be readily available to American readers, and in several cases there are gaps in the description which are to be filled in from these papers. A little study of the many tables will make the procedure clear, however. (Supplementary information may be found in [2] and [5].) The expressions for the output lines are simplified using the techniques in the first section of the paper; again only normal forms are used and the expressions are minimized singly.

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[5] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y., ch. 12; 1958.

Symmetric Switching Functions, Matrix Logic V—E. J. Schubert. (*Communications and Electronics*, pp. 1083–1087; January, 1960.)

The main, sparsely treated points randomly scattered through this paper seem to be:

1) The number of minterms of an ordinary symmetric function is given by the binomial coefficient ${}_pC_k$, giving the number of combinations of p variables taken k at a time. An ordinary symmetric function is one whose value is a one if and only if exactly k inputs are one. Also, each variable must occur as often as every other.

This is a special case of the more general rules given by McCluskey.[1]

2) There are two classes of symmetric functions, ordinary[1] and threshold. The latter are functions defined as one for k or more inputs equal to one.

This completely neglects symmetric functions other than threshold functions with more than one a-number.[2] A classic symmetric function left out, for example, is sum modulo two of three or more variables. Multiple nonconsecutive a-numbers are perfectly valid consequences of Shannon's definition of a symmetric function as one invariant to any permutation of the variables. The existence of such functions is completely implied by the rules given by McCluskey.[1]

3) Ordinary symmetric functions and threshold functions are mutually related, and one class may generate functions of the other class.

This statement is carefully worded, and together with the derivation given in the text, gives but slight hint to the limited nature of the statement. Properly qualified, the statement says very little.

4) A function of p variables with value one only if k inputs are one may be equivalent to another function with value one for exactly p-k variables. This is specialized in an equation showing the relations for threshold functions.

[1] E. J. McCluskey, "Detection of group variance or total symmetry of a Boolean function," *Bell Sys. Tech. J.*, vol. 35, pp. 1445–1453; November, 1956.
[2] C. E. Shannon, "A symbolic analysis of relay and switching circuits," *Trans. AIEE*, vol. 57, pp. 713–723; 1938.

This has been noted by Caldwell[3] in a more clear and preci fashion.

5) The intersection of two symmetric functions with differe a-numbers is zero.

Shannon[2] has pointed this out.

6) The intersection of a threshold and ordinary symmetric fun tion yields the latter only if the threshold of the former is higher tha the a-number of the latter.

This is an error. The exact opposite is true.

7) The union of two ordinary symmetric functions of the san variables is not a symmetric function because it does not satisfy M Cluskey's second rule.[1]

This is incorrect but understandable since the author ignor multiple a-number functions except threshold ones. However, suc slight mitigation is overridden by the completely erroneous stat ment that rule two is not satisfied. If all variables occur the san number of times in each of two functions, they will still be equal present in the union of the functions.

8) An expansion theorem for two symmetric functions in casca is given.

This has been done more generally by Grea.[4]

9) Cascaded symmetric switching circuits do not perform syr metric functions.

A simple counterexample is two AND's cascaded; each alone symmetric, and cascaded they form a symmetric function: $(A \cdot B) \cdot$

10) A chart method is proposed for detecting symmetric fun tions by mapping all possible a-numbers on a Veitch diagram. Plo ting the 1's of a function on this allows the careful observer note whether the 1's all fall on all instances of a particular a-nun ber. From this, synthesis for totally symmetric or for simple cases near-symmetric functions is meagerly described.

This method is similar to Caldwell's map method[5] initially, bu fails to use a Karnaugh map and loses the power of detecting pattern It falls considerably short of the methods of Marcus[6] and M Cluskey.[1]

There are a few other irritations in this short paper.

The author states out of context, and without explanation or fu ther reference, that the complexity of a symmetric function is cha acterized primarily by the term k (the a-number). The relationship not apparent.

The author consistently confuses the equation for the number c combinations of p things taken k at a time with a Boolean equatior

> "A proposition being true for any combination of p things take k at a time . . . ," or "Any function of p variables may be ex pressed by equation 1 . . ." where equation 1 is for pCk.

There is an error near the top of page 1085: Table III, line 1 should be referred to, not Table I, line 13.

The abstract and conclusion claim a method is developed fo logical design with symmetric functions and the merits of solid-stat logical elements performing threshold functions are revealed. But not only are the (questionable) merits of electronic devices perform ing symmetric functions not revealed, no logical design method no any attendant minimality for symmetric functions is discussed Methods for detecting symmetric functions (the key problem of find ing the variables of symmetry is ignored) are far removed from a gen eral logical design method for synthesizing arbitrary functions with few symmetric ones as basis within some sense of minimality. Thi broad and profound problem cannot be passed over or "solved" in s cavalier a manner. In the lone example of the appendix, the autho indicates either he does not feel restricted to symmetric functions i his synthesis, or for some reason uses symmetric notation onl partially.

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[3] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons Inc., New York, N. Y., p. 259; 1958.
[4] *Ibid*, p. 257.
[5] S. H. Caldwell, "Recognition and identification of symmetric switching func tions," *Commun. and Electronics* (*Trans. AIEE*, vol. 73, pt. II), pp. 142–146; May 1954.
[6] M. P. Marcus, "The detection and identification of symmetric switching func tions with the use of tables of combinations," IRE Trans. on Electronic Com puters, vol. EC-5, pp. 237–239; December, 1956.

Sequential Switching Circuit Theory and Iterative Circuits

Matrix Algebra of Sequential Logic, Matrix Logic III—E. J. Schubert. [*Commun. and Electronics* (*Trans. AIEE*, vol. 78, pt. 1), no. 46, pp. 1074–1079; January, 1960.]

This paper is the third in a series by the same author, in which a method of analysis is presented for deriving the behavior of networks of digital elements. The author purports to show how the matrix algebra developed in his first two papers[1,2] for combinatorial (*i.e.*, combinational) networks may be extended to apply to the analysis of sequential networks as well. A solution is also presented to the "synthesis" problem, which the author cites as the ultimate goal of the analysis, and defines to be, "A direct routine for synthesis of a network in order to produce a certain output sequence for a specified input sequence." Applied to the design of sequential logic, the author claims that his algebra has the advantage of "a complete and explicit representation of a net adaptable to computer routines." Also, "the simplicity of the matrix algebra in sequential logic appears to be advantageous over other presently known concepts."

No attempt will be made to describe here the notation and rules of the algebra. Suffice it to say that it bears little relation to conventional linear matrix algebra either in notation or postulates. Thus, a familiarity with the contents of the earlier papers is assumed and necessary for the understanding of this third one. The careful reader will also find it necessary to supply several missing assumptions, rules of manipulation, and proper interpretations of the symbolism employed.

With these assumptions, rules, and interpretations, the development is valid, and offers a procedure of analysis for determining the output of a sequential network, given the network and the input. (The initial state is assumed to be $00 \cdots 0$, and the input sequence finite.) This aspect of the analysis problem has never been considered to be a really difficult one, however, and was adequately solved in less intricate mathematical language by Huffman, Moore, and Mealy, references which were cited by the author. Other less completely solved aspects of the analysis question concerned with equivalence, inverse networks, dependence on initial state, effect of network cascading, etc., are not discussed here. While the procedure offered may conceivably have some advantage over the essentially tabular methods of Huffman, Moore, and Mealy for execution as digital computer programs, most users will favor less specialized language with a simpler set of rules. Consequently, it is difficult to agree with the author on the advantages he claims for his matrix algebra as a simple and complete analytical tool.

The "synthesis" problem which the author proposes to solve is a rather special case of the more general synthesis problems posed by Huffman, Moore, and Mealy. In the more general problem, the specifications require the network to transform whole families of input sequences into output sequences, not just a single input sequence into a single output sequence. Further, limiting assumptions which force the network to start in a fixed initial state and to operate with fixed-length input sequences are not usually imposed. Finally, when synthesis is identified with the logical design process, a constraint of economy is imposed: the network realization which satisfies the specifications must not be flagrantly wasteful of logical or storage elements. The solution for the special case treated in this paper is obtained by a process of "inversion" of the analysis equations. It is not clear whether the author realizes that this process is not unique. No mention is made of the state-assignment or state-reduction problems, and no criterion is proposed as to what constitutes a satisfactory realization. In any case, the recommended network form is highly redundant in storage elements. It consists of a register for serial-to-parallel conversion of the input sequence, followed by the usual model of a sequential network—a multi-output combinational net with some of the outputs fed back to inputs through delay elements or flip-flops. Thus, the synthesis method presented applies to a very special case, is not really complete, and leads to an unnecessarily wasteful realization.

The presentation builds up the algebra gradually through a consideration of successively more general network forms and a series of examples. The author observes that the examples are illustrative and elementary, and they do indeed help to explain the notation. They are unfortunately too elementary to reveal any virtues of the algebra as an aid to analysis or synthesis. Also, the necessity of some of the earlier assumptions in the paper is not too clear. For example, the restriction in Section 1, that all input sequences must start with a "1," seems artificial in view of the assumed synchronism (sampling over a fixed input word), and no direct use was made of the assumption in the balance of the exposition.

In short, the paper contains no original contributions to the theory or practice of sequential circuits, except the development of a specialized matrix algebra for the analysis of these circuits. The author's claims for the advantages of this new algebra for analysis and synthesis do not appear to be substantiated.

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A Theory of Asynchronous Circuits—D. E. Muller and W. S. Bartky. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University Press, Cambridge, Mass., vol. 29, pp. 204–243; 1959.)

Many designers feel that there are definite advantages (chiefly greater speed) in operating digital circuits asynchronously; however, because it is very difficult to design asynchronous circuits so that they will operate properly when constructed with practical devices most designs are basically synchronous. The authors address themselves to the problem of synthesizing suitable circuits; however, this paper is devoted solely to the development of mathematical models. Although the paper is over three years old at the time of review, very little additional development of these methods is available in published form (Bartky's paper[1] is available on a limited basis); this is undoubtedly due partly to the unconscionably long delay in the publication of the proceedings of the symposium. However, the reviewer knows of at least one rather complicated circuit which has been designed using these concepts.

The analysis is restricted to exclude any input changes and is closely related to analyses of "race conditions" in sequential circuits. An elaborate mathematical model is constructed for a very general class of acceptable circuits and a large number of new concepts are introduced. However, in order to simplify the analysis, further restrictions are introduced during the development. Thus, the original class considered (speed-independent circuits) requires only that the circuit move from its original state either to a unique state in which it is in equilibrium or to a buzzing condition in which it must remain indefinitely, *i.e.*, until an input is changed.

The restrictions to "semi-modularity" and finally "modularity" also allow this buzzing condition (and simultaneous changes of signals at two or more nodes) but restrict the possible sequences of changes. In essence they say that if the circuit can get into or out of a particular state by signal changes at either of two nodes, then the states corresponding to changes at both nodes exist and can be arrived at in a sequence of changes.

The authors introduce several concepts, in particular C state and C signals, which clearly may be useful in simplifying the description of all possible circuit actions. However, an evaluation of the significance of these tools will have to be made on the basis of their usefulness in circuit synthesis and must await further publications.

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[1] E. J. Schubert, "Matrix analysis of logical networks," *Commun. and Electronics*, (*Trans. AIEE*, vol. 77, pt. 1), no. 35, pp. 10–13; March, 1958. (Reviewed by E. J. McCluskey, Jr., IRE Trans. on Electronic Computers, vol. EC-8, p. 505, December, 1959.)

[2] E. J. Schubert, "Matrix synthesis of high-speed logic," *Commun. and Electronics* (*Trans. AIEE*, vol. 78, pt. 1), no. 41, pp. 4–8; March, 1959.

[1] W. S. Bartky, "A Theory of Asynchronous Circuits III," Digital Computer Lab., University of Illinois, Urbana, Rept. No. 96; January 6, 1960.

The Logic of Fixed and Growing Automata—Arthur W. Burks. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University Press, Cambridge, Mass., vol. 29, pp. 147–188; 1960.)

The first five sections of this paper are a continuation of a subject developed at the University of Michigan, Ann Arbor, beginning with the paper by Burks and Wright[1] The concept "fixed automation" (alias "finite automaton") is defined in the paper in a way that makes it almost synonymous with "logical net." It is only in the last, or sixth, section that the author takes up growing automata.

Although symbolic logic is used in the description of nets, the paper is meant to be read by practicing engineers rather than by symbolic logicians. By and large, the material is introductory in nature; there is no attempt to present difficult mathematical problems.

It is shown that finite input-output tables, of the kind which are known to be capable of describing switches (or combinational nets), are capable of describing those nets with delays that have no cycles. These tables, even for cycle-free nets, are impractical and the author considers it natural and necessary, at that point, to bring in information about the delay states of the net. This leads to state graph description, or, as it is characterized in this paper, the transition-table description. These are developed as matrices, and various operations on matrices are shown to be interesting. One of these is a test to find out which states are *inadmissible*, relative to a given state. (A state S' is inadmissible relative to a state S, if there is no sequence of inputs that will take the net from state S to state S'.)

An interesting contribution of the paper is the development of a concept of duality nets. The use of this concept in propositional logic is well known, and it is an easy matter to apply it to nets without delays. The technique used in the paper is to let the dual of a delay element be another delay element having the opposite time-zero output. Time zero being the initial instant of time, the output of the delay at time 0 is arbitrarily set at either 0 or 1. Of a set of two dual delay elements, one has an output of 0 and the other 1 at time zero. The reviewer finds it rather surprising that an interesting concept of duality results from this definition.

The discussion of growing (or potentially infinite) automata is rather brief. There are two kinds of concepts that are of interest: one is that of an infinite structure specified in advance, but having only a finite (but growing) amount of information at any time; the other is that of a growing structure that is finite at any time. In each case, it would seem to the reviewer, it is necessary to have the growth determined by rules, if the automaton is to be regarded as a deterministic device. An example of a computer having a growing serial storage is presented in detail.

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[1] A. W. Burks and J. B. Wright, "The theory of logical nets," Proc. IRE, vol. 41, pp. 1357–1365; October, 1953.

Pattern Recognition and Learning Theory

The Historical Development and Predicted State-of-the-Art of the General Purpose Digital Computer—C. P. Bourne and D. Ford. (*Proc. WJCC*, pp. 1–21; May 3–5, 1960.)

This paper presents "scatter" diagrams and graphs for the more usual quoted characteristics of about 300 computers. These collections of data are also discussed. Two graphs showing the number of different types of computers built per year and the total number of different types of computers developed to date are shown. There are eighteen scatter diagrams showing the number of addresses per instruction, the number of index registers per machine, the internal clock rate per machine, and the total memory size. Various figures of this type are plotted on the scatter diagrams against their year of development. The charts cover the years from 1944 to somewhat past 1960 and thus cover machines yet expected to be finished.

I was not able to notice anything unusual from looking at any of the data. Probably the most impressive thing is that over 250 different machines have been developed in a period of fifteen years, ove 80 per cent having been developed in the last seven years. The numbe of machines being developed per year has leveled off since 1952 a about 25 machines per year.

The scatter diagrams are so scattered that they do not really te very much that a person skillful in computers would not already b pretty well aware of. They show that the predominant number of ma chines uses single-address instructions. They show that most ma chines with index registers tend to have about ten such register The rest of the diagrams concerning operating times, the number c bits per word, and the size of the memory are spread over such wide range (usually more than three to one) that no conclusions ca really be drawn. This is not actually very surprising because th number of bits in a memory (or word) does not really say muc about the usefulness of the memory unless the speed of the memor and the nature of the instructions used with the memory are know With core memories it has been possible to make machines with le than 3000 bits of memory which compete with drum memories cor taining five and in some cases ten times as many bits.

To make meaningful comparisons one needs to plot figures o merit for the various machines rather than the raw data as has bee attempted in this paper. Even then, a statistical approach to such new and dynamic situation may not be very meaningful. In th question of pulse rates, for example, I know of machines whic execute as few as two logical (AND or OR) operations per pulse tim while in another machine (under development) that I am familia with there can be as many as twenty-four logical operations betwee pulse times. Thus a pulse rate may make an error of five or ten to or in expressing the effective speed of the circuit. This matter is furthe complicated by the fact that some machine designers speak of puls rate as a period between the repeated impulses of a given clock phas while other designers express the clock rate as this figure multiplie by the number of clock phases used.

Two of the scatter diagrams, the number of memory speed leve and the type of high-speed memories, confirm what has been fairl obvious to most people in the field: 1) most machines have not gor beyond one or two levels in their memory hierarchy at the preser time, and 2) while machines were largely designed with drum memo ries five years ago, most machines are now being designed with son form of core memory.

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Communications Within a Polymorphic Intellectronic System—G. P. West and R. J. Koerner. (*Proc. WJCC*, pp. 225–227; May 3–5 1960.)

This expository paper is concerned with the RW-400 systen which is made up of a highly flexible interconnected network of ind vidual general-purpose computer modules, auxiliary storage device (buffer modules), and input-output modules. The authors ably de scribe the salient features of the Central Switching Exchange whic affords communication between the various modules of the systen The switching exchange consists of transfluxor crossbar switches tha can provide information transfer paths in either direction betwee many different pairs of modules simultaneously. A separate table look-up transfluxor memory device called an interrogation modul is employed, which permits the programmer to specify, for intercon nection, the various modules in the system by means of symboli tags instead of by unique identification numbers determined by th physical connections of the modules to the crossbar switches.

The authors touch upon some of the interrupt features, which ar all-important for efficient utilization of a computer network. On of these features is the use of a digital clock whereby an interrup occurs at a predetermined time, but whether this requires knowledg on the part of the programmer of the times for various modules t complete various tasks is not stated. How the interrogation modul is used to simplify the problem of interrupt-communication withi the system is described rather sketchily, and it seems that the im portance of the topic would warrant a more comprehensive treatmen

It is indicated how the accessibility of certain crosspoints of th switching exchange is restricted for the sake of program checkin and how identical switch address tags can be used concurrently b two independent programs.

It would appear that the idea of a "telephone exchange" such as he authors expound for use in a computer network is a fruitful one nd that it represents a valuable contribution to the design technol- y of computer systems.

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orizons in Computer System Design—Walter F. Bauer. (*Proc. VJCC*, pp. 41–52; May 3–5, 1960.)

The paper is primarily concerned with trends in the organization f computers and in methods for the development of system designs. s an introduction to these subjects, the author touches lightly on rends in circuit and component development, programming tech- iques and computing system applications. "Information systems" re singled out as the computer application area of the future. Such ystems are characterized by continuous information and control xchange among humans, and computers and other devices.

As a result of development of the field of "information systems" pplications the author visualizes the following organizational re- uirements for the computers of the future. The computers should ave an internal control structure that will provide for versatile ntegration into a multicomputer and multiprogram system. The ommunication and control between men and computers operating n an "information system" should be improved. These systems hould be designed to make better use of their large memories. Com- uters should be designed so they can be adapted to the problems of a ustomer. The author offers modular organization as one basic solu- ion to most of these organization requirements. In addition, he ecommends internal control provision for a hierarchy of system ontrol and for microprogramming.

Most of the suggested organization requirements are provided in arying degrees and in different ways in the new computers that are xpected to be operating in the next few years. However, the paper nly cites two examples of these trends in computers other than the RW-400.

Queueing theory and computer simulation are two techniques that re suggested for system design analysis. The paper presents and iscusses a process flow program for information systems design and process flow diagram for application evaluation. These techniques or analysis and methods for design and evaluation have been and re being used in the development of the new generation of computers. ncreasing effort is now going into this area of system design because f the pressure of commercial competition and because of the com- lexity of the over-all systems in which the computers must operate.

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Organization of Computer Systems—The Fixed Plus Variable Structure Computer—Gerald Estrin. (*Proc. WJCC*, pp. 33–40; May 3–5, 960.)

In view of the present expectation that microminiature, milli- microsecond, two-for-a-penny logical components are just around the orner, it is of the utmost importance that radical changes in the logi- al organization of digital computers be studied energetically. Radical hanges will be especially important if arithmetic and logical ele- ents become as small and cheap as memory elements, and par- icular attention will need to be given to letting very many arith- etic units share a memory.

The particular point of attack discussed in this paper is that of computing system which can be readily reorganized (manually or utomatically) into one of a variety of problem-oriented special-pur- ose systems. It is assumed that an important set of problems exists or which problem orientation of the computer system more than vercomes losses in performance caused by built-in reorganizability.

More specifically, the subject system would consist of a fixed achine plus an "inventory of substructures." The fixed machine ould be at least sufficient to permit communication with humans in a satisfactorily sophisticated language. It would also contain complexes believed useful to most problems, and would grow in this respect when and if experience so indicated.

A detailed discussion is given of how the time necessary to evaluate a polynomial depends upon the number of multipliers available. A problem in combinatorics is mentioned in which computing time could be reduced by several orders of magnitude by an accumulator capable of variable radix addition. Unfortunately, no example is given of an actual problem whose solution would obviously be valuable and which would benefit from a special-purpose computer.

The idea of a general-purpose system which can be arranged to constitute a variety of special-purpose systems seems well suited to the important task of evaluating the potential power of special-purpose digital computers. It is to be hoped that concrete demonstrations of this power will soon be forthcoming.

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Digital Computer Principles—book by Wayne C. Irwin. (D. Van Nostrand Co., Inc., Princeton, N. J.; 1960. 314 pages.)

This is a good, self-contained, up-to-date introduction to the engineering principles involved in present-day general-purpose digital computers. It is written at the level of a mature industrial technician or advanced college undergraduate, and does not prerequisite any specially related technical background. It is quite complete for its relatively short body of textual material, interesting to read, and provocative enough at points to stimulate even the professional. The author's secrets are his talent for precision in a flowing style, a usually trenchant exposure of introductory level principles, and a highly complementary use of reading matter and charts, diagrams, and sketches. Except perhaps for one section, the book has the rare virtue among its kind of developing, with a minimum of ambiguity, both the language and to a significant extent the process of a large body of technology all within a short span of text. This book arose out of an industrial training course, but it seems well qualified to serve also as a self-study or undergraduate college text.

The over-all work is divided up into eleven sections covering, in order: methods of computation, logic, the mechanization of logic, memory systems, timing, the mechanization of arithmetic, control, input-output equipment, programming, the reduction of errors, and present trends. The book moves constantly from details towards the synthesis of a general system, which is probably the best method in an introductory work intended to appeal to a wide diversity of backgrounds.

The author has not included any problems. This is unfortunate because otherwise the book seems especially well arranged to make its ideas viable, a crucial characteristic for the class of readership it probably will enjoy. Also, a great deal would have been added if a good list of references had been included at the end of each section, instead of a single, integrated, and just-adequate bibliography at the end of the text.

In my opinion the book has one major feature that is rather dubious, the explanation of which follows. The author begins the book with a discussion of number systems and ways of doing arithmetic in machines. Then he goes on to say that since arithmetic is "logical," if a "digital computer is to solve arithmetic problems it must behave in a logical manner." He aptly points out the absence of precision in everyday English, and advances symbolic logic as the language with which computers must be designed and analyzed. Next come the truth tables and their concrete interpretation in the form of switching circuits. Then in Chapter 10 the focus of attention is turned from symbolic logic to the "Basic Notions of Boolean Algebra" with the statement that "there is a form of symbolic logic which can be applied with great advantage to the design of computers . . . Boolean algebra." Ten pages and one chapter later, Boolean equations are derived from truth tables and the usual remaining switching circuit aspects of Boolean algebra are taken up.

Now my feeling is that there is no justification for mentioning anything about symbolic logic at all. A straightforward exposition of the 2-valued Boolean algebra, or simply "switching algebra," is entirely sufficient, and furthermore, obviates lengthy commentaries on the rather exhaustive and slippery notions that one first encounters

in decent applied logic. Granted, the combined logical-algebraic approach adds an aspect of inherent interest. But if the logic is underdeveloped to save space, there is too much unnecessary vagueness that crops up in the backwash of transitions between the two areas. The book's use of logic does not seem to cause any real harm, because regardless of any significant confusion that might develop, the essential points all seem to straighten themselves out by Chapter 11, in which Boolean equations are derived from truth tables. It's just that the purpose of the book does not seem especially to merit the inclusion of a discussion of logic.

My final remark is that it is good to see a concise and instructive section on programming in an otherwise design-oriented computer book. The section is not long, but clearly points out the need for the computer engineer to know something about program structures and the relation between internal and external computer languages.

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A Built-In Table Look-Up Arithmetic Unit—R. C. Jackson, W. H. Rhodes, Jr., W. D. Winger, and J. G. Brenza. (*Proc. WJCC*, pp. 239–250; May 3–5, 1960.)

The Arithmetic Unit described in this paper features the novel combination of a translation-type arithmetic with the translation ability of a random access memory. This system operates serially, taking a single decimal digit at a time from each operand to perform addition, subtraction and multiplication. The instruction determines the stored arithmetic table to be used (*i.e.*, addition or multiplication) by inserting a code into the first three digits of the memory address register. The digits, one from each operand, are used to make up the other two digits of the five-digit address. The result of the desired operation is then read from the table stored in the core memory. The arithmetic unit operating serially imposes no limit on the size of the operands and the result, the only restrictions being the memory space that can be allocated for these numbers. This system, by virtue of the fact that it was used in an engineering model of the IBM 1620 computer, is more than just a new idea. However, some of the limitations of such an organization should be mentioned.

The speed of this system, which is not mentioned in the paper, will be limited by the memory. Four memory cycles are required to add two decimal digits. Therefore, present memory techniques will limit this sytem to medium or slow speed computers.

The arithmetic operations use five memory address registers of at least twenty-five bits. If these registers were transistor-resistor logic registers (which they are not), one register would be equivalent to a single decimal digit adder (or subtracter). This comparison, although artificial, implies that the low cost depends on inexpensive registers as well as the table look-up mode of operation.

The paper presents a well-organized description of an interesting Arithmetic Unit, and what seem to be limitations today may not exist in the future.

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Use of a Computer to Design Character Recognition Logic—R. J. Evey. (*Proc. EJCC*, pp. 205–211; December 1–3, 1959.)

In a scheme for recognizing characters printed with magnetizable ink, the characters first pass an ac writing head which induces a field in the ink. Next, this field is sensed by a thirty-channel reading head in which channels ten apart are summed, so that the output is a set of ten time-dependent voltage waves. The outputs are sampled, quantized into seven pulses each (the font's strong leading edge provides horizontal registration) and stored in a 10×7 trigger matrix. To avoid the vertical registration problem, the patterns are tested for in ten vertical positions and the corresponding character trigger is set if the character is found in any. If two character triggers are set the pattern is rejected.

This paper describes the application of a digital computer to design the "logics" used to test the 10×7 trigger matrix for the fourteen characters to be recognized. The design is not automatic. The computer is used for testing logics designed by people and for recording various data of interest to the designers. It was also used to prepare from a set of ideal patterns (on a much finer grid) sets of patterns capable of incorporating the effects of both intentional variations of apparatus parameters and random aberrations in printing and reading. Logics were tested both against the theoretical noisy shapes produced by this program, and against real-life shapes as read on a hardware model.

The logics were designed by hand, with repeated trials, starting from a set of "sure" bits for each character. These are bits found to be effective for recognizing that character. By cross-testing against the other characters, bits not effective in distinguishing the given character from others are eliminated from the set. After each modification of the logics they were tested against the theoretical and real-life shapes, performance being tabulated and certain errors resulting in detailed print-outs for the designers to examine. The process stops when the designer feels satisfied.

As noted by the author, use of the computer is restricted to simulating noisy character samples, handling the mass of data involved in evaluating logics and keeping the progress records of a practical task.

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Symbolic Logic in Language Engineering—H. M. Semarne. (Published in 1960 as Engineering Paper No. 980 by Materials Research and Process Engineering, Douglas Aircraft Co., Santa Monica, Calif. 27 pages, 8 illustrations, 8½×11. Presented at WJCC, San Francisco, Calif., May 2–6, 1960.)

"It is the object of the present paper to show how symbolic logic, as a tool, can be introduced gradually into the problems of information storage and machine searching and translation . . . " to quote from the author. The symbolic logic methods described depend upon fragmentation of a text into elements or propositions such as a = "the hydraulic fluid is an organic phosphate ester." The message of the text is then expressed in a multi-argument logical function of such elements. These logical functions are claimed to be useful for information retrieval, analysis of data, and mechanical language translation. It should be noted that these general methods of logic in language for "data analysis" date back at least to Lewis Carroll. Also, for the past two years, Thyllis Williams at ITEK Corporation under NSF grant has been attempting to apply similar logic methods to retrieval. The author mentions the use of such interesting sounding methods as "truth matrix techniques," "group theoretical relations," "probabilistic weighting," and other devices for using or dealing with the logical functions. Unfortunately, the author does not give sufficient explanation to permit a reader to verify the appropriateness of these devices or to make use of them for the logic techniques described. Most of the paper is devoted to information retrieval, which is the primary area of the reviewer's competence. Here, where the author's presentation could be followed, the methods appeared to have doubtful utility for a variety of reasons. One important reason is that his method necessarily depends upon first preparing an exhaustive list of all the propositions that might ever be used. The author devotes only a few lines to this matter, and lightly dismisses it before noticing that such a list, being made of finite strings of words from a finite vocabulary, is nevertheless nondenumerably infinite. Thus, as a practical matter, such a list cannot be prepared. Neither does the author realize that such word-string propositions are incomparably more complex and intractable for use in retrieval than individual words or the more sophisticated but easier to use descriptors. If this problem of the propositions cannot be resolved, then the mere introduction of logic functions, which must be based on such propositions, cannot be of much use. Unfortunately, the paper abounds in loosely-worded provocative statements and allusions, which would be most interesting if true, but which are not further explained.

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Digital Computer Systems

Automatic System and Logical Design Techniques for the RW-33 Computer System—T. A. Connolly. (1960 IRE International Convention Record, pt. 2, pp. 124–132.)

The R-W Logic Simulation Program—H. Adler, H. Jacobs, and J. Katz. (AIEE Conference Paper CP60-1063, presented at the AIEE Pacific General Meeting, San Diego, Calif., August 9–12, 1960.)

In spite of the differences in the titles of these two papers, they cover the same subject matter. The title of the latter is the more accurate. In the former paper principal application is to the RW-33 computer and in the latter paper it is the RW-400, but the subject matter of both papers is applicable to any computer which is designed in a certain systematic manner.

The possibility and need for using computers to assist in the design of computers has long been recognized. However, as yet very little has appeared in the literature which reports actual achievements in this direction. As recognized by the authors, the achievements reported in these two papers are far from the ultimate answer to computer design problems, but the papers nevertheless report an important and highly useful first step.

The authors do not claim to have "designed" one computer by means of another. Instead, what they have done is to develop a scheme for using a computer to check the logical design of another computer before this other computer is built. This result is accomplished by developing a computer program to simulate the interconnections of logical elements (AND circuits, OR circuits, flip-flops, etc.) of the computer under study.

There are several important steps to the checking process. First, the computer being designed is represented by a set of logical (Boolean) equations. Second, these equations are punched into cards with a suitable notation being used to represent the logical functions. Third, the data from the cards are entered into a computer which compiles from these data a "logic simulation" program. Fourth, the simulating computer causes appropriate initial conditions (initial settings of bistable elements) to be assumed for the simulated computer, and the simulating computer then proceeds through one or more time steps of operation of the simulated computer. Apparently, the number of time steps usually employed was the number required to execute one instruction in the simulated computer. Last, the simulating computer compares the conditions of the simulated computer at the end of the run with the conditions that the designer intends. If the comparison checks, it is assumed that the logical design is correct. If it does not check, the conditions of each bistable element can be printed to give the designer clues to the source of the error in logical design.

The authors point out that their logic simulation program can also be used to precheck programs as well as logic design. All that is necessary is to use a suitably large number of time steps of simulation. Program checking of this kind was actually done for a certain small earlier machine, the RW-41, but it was pointed out that the complexity and size of the RW-400 was too great for program checking of this kind to be practical even with an IBM 709 available. However, it should be observed that the simulation of one computer by another computer on an instruction-by-instruction basis is now common practice and appears to be a much more efficient means to check programs than to simulate detailed logic functions.

It should be understood, of course, that the actual simulation program is a very long and complex thing, and the authors do not attempt to present all of the details. An engineer or group of engineers wishing to prepare such a program of their own would get from the papers only a general outline of ideas and the assurance that productive results are obtainable.

Inasmuch as the first step in the logic simulation process is the preparation of logic equations, it follows that the usefulness of the scheme is dependent on the possibility of representing the computer by logic equations. Most presently successful commercial computers, for example, have much "hodge-podge" in their logical design, and it is difficult, if not impossible, to represent such computers by sets of logic equations. It will be interesting to observe, as time passes, if the need for logic simulation forces a more complete adoption of the logic-equation technique by those companies which so far have made only limited use of it.

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Two Theorems of Statistical Separability in the Perceptron—F. Rosenblatt. (Mechanization of Thought Processes, Natl. Phys. Lab. Symp. No. 10, Her Majesty's Stationery Office, London, Eng., pp. 421–450; 1959. In the U. S.: British Information Services, New York, N. Y.)

This paper purports to prove two theorems on the steady-state behavior of a class of perceptrons. While it may be unfair to demand at this stage of development of the perceptron a rigorous mathematical exposition, it is not unreasonable to ask for care in the presentation of mathematical ideas. There is such a conspicuous lack of care in defining terms and stating theorems that it casts a serious doubt (at least in the reviewer's mind) as to whether there is any nontrivial content in this paper.

The principal "results" are embodied in two theorems and their corollaries are stated but not proved. The author "proves" the theorems by a consideration of two special perceptrons. This causes the reader to wonder whether or not there exist more substantial examples. As statements are made without proof in the discussion, it is impossible to determine the veracity of the end results. In the reviewer's opinion there is little (if any) mathematical content in this paper.

In sharp contrast, we direct the reader's attention to a report by Keller[1] which shows the relation of the perceptron to general finite automata. As Keller remarks, there is too much emphasis on the analogy to human nervous systems with the subsequent morass of psychological and physiological terminology which tends to obscure the nature of the basic mathematical problem.

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[1] H. Keller, "Finite Automata, Pattern Recognition and Perceptrons," AEC Computing and Appl. Math. Center, Inst. of Math. Sciences, New York University, N. Y., March 1, 1960.

Self-Organizing Systems: Proceedings of an Interdisciplinary Conference—M. C. Yovits and S. Cameron, Eds. (Pergamon Press, New York, N. Y.; 1960. ix+322 pages.)

This paperback book represents the official proceedings of an interdisciplinary conference on the subject of cognitional systems that was held in Chicago on May 5–6, 1959. The main body of this well-edited and well-reproduced work consists of 13 technical papers (averaging better than 20 pages apiece) contributed by 15 eminent researchers whose background includes the fields of philosophy, electrical engineering, physiology, and psychology. In addition, the book terminates with the text of an interesting after-dinner speech of a technical nature by Uttley concerning the mechanization of thought processes. Each paper is followed by a controlled discussion from among the nearly 400 people that attended the conference. The papers can be broken down into four ill-defined categories as follows: 1) perception of the environment (4 papers), 2) effects of environmental feedback (3 papers), 3) learning in finite automata (3 papers), and 4) principles of self-organizing systems (3 papers). The compendium contains two panel discussions with audience participation. The first of these serves to correlate the papers of 1) and 2), while the second serves to correlate the papers of 3) and 4).

Now the reviewer will treat the papers in what he considers to be a decreasing order of fundamentality—the most basic paper being discussed first. In no sense is this meant to de-emphasize the engineering significance of the last few papers to be mentioned. Because of certain incomparabilities pertaining to the abundantly complex relations between various papers, some of them will be discussed only in relation to others. Since the reviewer wishes to be fair to authors and readers, he points out that this arrangement is in no sense unique. Discussion of one paper in respect to another does not necessarily imply that the two are of the same stature.

Gordon Pask's paper, "The Natural History of Networks," falls into category 4) of the papers. He deals with, among other things, two very useful principles associated with self-organizing systems. These sound principles are: 1) in order to utilize the self-organizing nature of a system one must make certain compromises and become a "natural historian" (*i.e.*, one who makes comments on gross observed *interaction* between networks rather than comparing the

local physics of the individual networks), and 2) in synthesizing networks, which are to display self-organizing characteristics, there are conceptual difficulties which essentially force one to become a natural historian when looking at these constructed models. Such difficulties come to light only in the physical model. Both principles are well known in the social-humanistic sciences, but Pask has drawn an analogy that is useful to the more physical of sciences. From the ecological point of view, it seems clear to the reviewer that one cannot overestimate the importance of pure interactive processes—such is much of the business of human communication. In spite of its mathematical obscurity, the Pask paper deserves careful consideration from the engineering community.

In relation to Pask's paper, it is appropriate to consider D. T. Campbell's paper, "Blind Variation and Selective Survival as a General Strategy in Knowledge-Processes," which falls into category 3) of the papers. This cybernetic-minded psychologist, who is a proponent of the phenomena of serendipity, is of the very old jointschool of philosophy and psychology which believed, mistakenly, that a prerequisite to a study of epistemology should be a study of knowledge processes of the mind. In fact, the pragmatic philosophy of C. S. Peirce helped save much of philosophy from the sterilizing effect of psycho-philosophy. However, the study of knowledge processes has been a rich and fertile source of information for psychologists. Campbell studies self-organizing systems by using an analogy to Darwinian evolution, which in its turn describes an extension of quite ancient politico-economical ideas to biology. But it seems to the reviewer that Pask's treatment of self-organizing systems involves a certain analogy to Lamarchian evolution of the general nature of habit-taking. Hence a certain contrast exists between these models.

H. von Foerster's paper, "On Self-Organizing Systems and Their Environments," [category 1)], will also be considered in relation to Pask's paper. One of von Foerster's basic assumptions, also held by Pask, is that energy and information are weakly-coupled phenomona. In his *reductio ad absurdum* proof (questionably based on thermodynamic principles) of the nonexistence of self-organizing systems, von Foerster shows, rightly, the importance of environmental effects. The reviewer points out that, contrary to von Foerster's example on page 35, there is nothing logically *wrong* with a planetocentric system of astronomy. Acceptance of the heliocentric system is purely a matter of applying Ockham's Razor.

The reviewer considers the second most fundamental paper to be W. S. McCulloch's paper, "The Reliability of Biological Systems," which falls into category 4). McCulloch extends the results of an earlier paper, "Agathe Tyche,"[1] which deals with some aspects of errorology by means of probabilistic logics (*i.e.*, a calculus in which a function can be uncertain even when its arguments are not uncertain). Equally important, he describes a number of relations between various kinds of error-reducing redundancies (*e.g.*, redundancy of code, redundancy of channel, redundancy of computation and redundancy of potential command). The concept of the redundancy of potential command is closely related to Selfridge's "Pandemonium."[2]

The third most fundamental paper, "Computation, Behavior and Structure in Fixed and Growing Automata," was written by A. W. Burks, to whom Peircians owe so much. This paper falls into category 4) and deals exclusively with deterministic automata (*i.e.*, Turing machines). Burks interprets some of the results of recursive function theory in terms of Turing machines. Then he presents some results on "growing automata," which are concerned with an alternate definition of self-reproducing automata as given by von Neumann.[3] However, his definition departs from known biological characteristics (*e.g.*, transit delays are lacking), and each cell of his has stronger primitives than von Neumann's more basic cell.

In respect to Burks' paper, the reviewer would like to mention three papers dealing with interesting deterministic models for learning processes. There is B. G. Farley's property-class model, which appears in his paper, "Self-Organizing Models for Learned Perception" [category 1)]. The details concerning the general problem solver of A. Newell, J. C. Shaw, and H. A. Simon are contained in their paper, "A Variety of Intelligent Learning in a General Problem Solver" [category 3)]. P. M. Milner's "learning" synapses are treated in his paper, "Learning in Neural Systems" [category 3)].

Next we will consider two statistical models for perceptual learning. F. Rosenblatt's paper, "Perceptual Generalization Over Transformation Groups" [category 1)], is one of the models for learning backed up by considerable experimental data (Farley deals also with much data). The work of Rosenblatt is certainly to be encouraged, although the reviewer believes that his approach is somewhat short-sighted. W. K. Estes' paper, "Statistical Models for Recall and Recognition of Stimulus Patterns by Human Observers" [category 1)], deals with simple pattern recognition by humans under laboratory conditions. A rather simple-minded statistical analysis of the data is undertaken by him. The last three papers deal with cybernetic aspects of biological structures. G. H. Bishop's paper, "Feedback Through the Environment as an Analog of Brain Functioning" [category 2)], deals with establishing that the complexity of organization in tissue should correlate with flexibility of behavior. S. Goldman's paper, "Further Considerations of Cybernetic Aspects of Homeostasis" [category 2)], treats of topics in the application of control system theory and information theory to a study of homeostasis. R. Auerbach's paper, "The Organization and Reorganization of Embryonic Cells" [category 2)], considers the process by which embryonic mechanisms are replaced by more sophisticated mechanisms of control and communication.

The reviewer has observed only three trivial typographical errors in the book, and he heartily recommends it to younger engineers as a primer for "the new trend."

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A Self-Organizing Binary System—Richard L. Mattson. (*Proc EJCC*, pp. 212–217; December 1–3, 1959.)

The number of technical papers dealing with various aspects of the pattern-recognition problem continues to increase in a more or less impressive if not gratifying manner. This paper, although the title does not readily suggest it, is concerned with pattern-recognition processes in which the pattern classes are determined by the so-called "linearly separated" Boolean functions.

The logical device upon which Mattson's model is based separates binary input combinations of the form $I_1 I_2 \cdots I_n$ into one of two classes according to whether the expression

$$T + \sum_{i=1}^{n} w_i I_i$$

is positive or negative, where T is an adjustable threshold and the w_i values are adjustable weighting factors. A useful geometrical interpretation is given in terms of the hyperplane

$$T + \sum_{i=1}^{n} w_i I_i = 0,$$

which divides the n-dimensional Boolean input space into two sets of points. By means of an iterative trial-and-error adjustment procedure, the values of T and the w_i, which determine the position and slope of the hyperplane, can be varied, and a mapping function which maximizes recognition performance can be obtained.

The author shows in a series of computer simulations that these mappings are useful in certain pattern classifications. Various printed characters represented on 5×5, 7×7, and 5×10 arrays of binary inputs are successfully distinguished in the presence of small amounts of complementation noise. Interestingly enough, the model also seems to work quite well in the final demonstration, that of distinguishing waveforms in noise, even though the waveforms are represented as sets of binary-coded rather than reflected-binary-coded numbers.

The paper is generally well organized and presented. It is unfortunate that the reader who wants to go into Mattson's work in more detail will find that the references given are not widely available.

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[1] W. S. McCulloch, "Agathe Tyche," Mechanization of Thought Processes, Natl. Phys. Lab. Symp. No. 10, Her Majesty's Stationery Office, London, Eng.; 1959. (Review by H. A. Helm to appear in the March, 1961, issue of these TRANSACTIONS.)

[2] O. G. Selfridge, "Pandemonium, a paradigm of learning," Mechanization of Thought Processes, Natl. Phys. Lab. Symp. No. 10, Her Majesty's Stationery Office, London, Eng., pp. 513–531; 1959. (Reviewed by O. Firshein, this issue, p. 525.)

[3] J. von Neumann, "The general and logical theory of automata," in "The World of Mathematics," Simon and Schuster, Inc., New York, N. Y., vol. 4, pp. 2070–2098; 1956.

utomatic Control by Visual Signals—W. K. Taylor. (Mechanization Thought Processes, Natl. Phys. Lab. Symp. No. 10, Her ajesty's Stationery Office, London, Eng., pp. 842–855; 1959. the U. S.: British Information Services, New York, N. Y.)

The first third of this paper is given to a compilation of highly sirable goals for visual pattern recognition and control systems. is claimed that the techniques to be described in the paper will ovide useful outputs for handwritten and printed input material. ch methods of machine synthesis, it is said, may read books, trans- ting the printed version to a spoken version as a prosthetic aid to e blind. Further, not only will this system recognize such patterns efully, but it may also be taught so to perform.

These are fine desiderata; unhappily they never seem to be real- ed in the balance of the paper.

The described system proposes an algorithm to classify simple ne-drawings by evaluating functions which are derived from spa- ally quantized representations. Its philosophy is based on the com- tation of a function y which is simply related to the average value all the quantized input signals and to the set of all signals possible the array. Maximized values of y are claimed to lead to unique entification of patterns. Careful examination of the system reveals at what is being described (but is by no means apparent) is a varia- on of an old theme, template matching.

The proof given is for a restricted case in which all the nonzero put signals are equal. This is clearly a binary situation which un- rtunately has no relevance to the two examples having nonequal gnals which are given just prior to the proof. This irrelevance is not pinted out; one must discover it. Furthermore, the concluding re- arks plainly state that the value of this system resides in the fact at it does not deal with binary signals.

The analysis presented seems to be more involved than its results arrant, and the expression preceding equation (2) is obscure at best. he expression following (2) appears to be in error; the quantity $-m/(m-j)$ should read $1-j/(m-j)$.

It is claimed that "all classified input patterns of equal intensity ould give maximum y signals of equal amplitude. . . . " It is not ade clear what is meant by "equal intensity." If one makes the easonable assumption that the sums of intensity values are the same or different input patterns, then working out a simple example ased on the required calculations denies the statement. If it is as- med that "equal intensity" means identical signals, then the case is ivial.

This paper is not overburdened with coherence, and it leaves ne impression that something significant has been said, but one is at loss to say just what.

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andemonium, A Paradigm for Learning—O. G. Selfridge. (Mechani- ation of Thought Processes, Natl. Phys. Lab. Symp. No. 10, Her Majesty's Stationery Office, London, Eng., vol. 2, pp. 513–31; 1959. In the U. S.: British Information Services, New York, N. Y.)

"Pandemonium" is a model which can adaptively improve itself to andle certain pattern recognition problems which cannot be ade- uately specified in advance. Examples of patterns taken from some et are presented to the model, and the model is informed each time as o which pattern has just been presented. After some time the model ould guess correctly which pattern is being presented.

Pandemonium handles data in a parallel manner and consists of n assembly of quasi-independent modules arranged on four levels f processing: a data-storage level (image demons), a level on which mputations are made on the data by "computation demons," a level f "cognitive demons," each of which weighs the evidence provided y the computation demons and "emits a shriek," and a decision evel consisting of a decision demon which selects the cognitive emon which "shrieks the loudest."

Several kinds of adaptive improvement are discussed. "Feature eighting" consists of altering the weights assigned to the computa- on demons by the cognitive demons so as to maximize the score of ne entire Pandemonium. The generation of new computation de- ons (sub-demon selection) is performed after the feature weighting peration has done its best. Then the computation demons with low orths are eliminated, and new computation demons are generated by "mutating" the survivors and reweighting the assembly. Mutating is done by altering, at random, the parameters of one or more computation demons. "Conjugation," another way of generating computation demons, is performed by combining the output of two "useful" computation demons, say A and B, into one of the forms $A \cdot B$, $A \vee B$, $A \cdot -B$, etc. In addition to the feature weighting and mutation types of adaptation, a cursory exposition of organizational adaptation and a suggestion for unsupervised operation is given.

The Pandemonium concept has been applied to the problem of distinguishing dots and dashes in manually keyed Morse code. At the time of the symposium the program was being run on the IBM 704, and only partial results were available.

The most important features of the Pandemonium program are the emphasis on parallel-data processing, the use of an assembly of quasi-independent modules for modification purposes, and the willingness to build up complex structure by means of an empirical, evolutionary technique.

This scheme, as most other pattern-recognition schemes, should be quite dependent on the initial choice of pattern characteristics (computation demons). Furthermore, the generation of new computation demons by the conjugation process seems to be too limited and narrow a tool for the generation of *new* (independent) and *relevant* characteristics when old ones prove insufficient.

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Circuits

Selected Semiconductor Circuits Handbook—Seymour Schwartz, Ed. (John Wiley and Sons, Inc., New York, N. Y., pt. 6, pp. 6.1–6.64 and pt. 7, pp. 7.1–7.51; 1960.)

Part 6 of this new handbook is devoted to switching circuits, while Part 7 is concerned with digital logic circuits. In the preface the editor states as a reason for the book, "The purpose of this handbook is to make available to the semiconductor circuit engineer a large selection of well-designed and reliable circuitry, as well as a comprehensive design philosophy text, as an aid in the design of circuits for electronic equipment and systems." Each part of the book is split into two sections. The first section is concerned with basic design problems, while the second section contains a group of specific circuits in which all circuit parameters are shown and, in some cases, some operational data are given. Each circuit also has a short write-up describing the various features of the circuit.

The first section of Part 6 is concerned with switching circuit design problems. A transistor equivalent circuit and a grounded-emitter collector characteristic is shown along with various dc parameter relations which are necessary for design. Included is an expression showing the temperature dependence of I_{c0}. Next the Ebers and Moll equations for turn-on, turn-off, and storage times are given and there is a short discussion of these equations. This is followed by a discussion of the design of a saturating Eccles Jordan flip-flop and next the design of a nonsaturating Eccles Jordan circuit in which the transistors share a common emitter load. Two nonsaturating inverter circuits are shown. In one the collector is clamped in both directions; the other remains out of saturation because of a feedback diode from collector to base. A complementary emitter follower is also shown and discussed. The next topic concerns triggering flip-flops and three triggering methods are discussed.

Two blocking oscillators are shown. In the first, the transistor saturates, and collector-to-base feedback is used. Expressions are given for base and collector currents and pulse width. The second blocking oscillator uses emitter feedback, and the transistor is clamped out of saturation. This section closes with an illustration of a DCTL flip-flop and a short discussion of DCTL circuitry. The design of DCTL circuitry is covered in Part 7. Also presented is a short discussion of *p-n-p-n* switches. The volt-ampere characteristic of a *p-n-p-n* diode is shown, and a basic monostable and bistable amplifier are illustrated.

The second section of Part 6 contains twenty specific circuits submitted by different designers from many different laboratories. Included are eleven flip-flop circuits, five multivibrators, three blocking oscillators, two inverters, a Schmitt trigger, a DCTL clock source, and a differentiator and pulse-shaping circuit. Each circuit has a short write-up, and all circuit parameter values are shown.

The first section of Part 7 of this book discusses logic circuitry. Diode- and emitter-follower AND and OR circuits are shown and

briefly discussed. Next, the DCTL parallel and series gates are shown, design problems are discussed, and design equations are shown. The problems of the DCTL series gate are also discussed. This is followed by a discussion of the resistor transistor TRL circuit. Design equations are included. Also shown are diode-transistor gates which are similar to the TRL circuit, except that parallel diode inputs replace parallel resistor inputs. One of the diode-transistor gates illustrated employs a transformer for coupling a clock pulse. The last AND/OR circuits discussed in this section are the complementary current switching circuits.

The last part of this section describes and illustrates the logic of some binary counters and shifting registers. Specifically, a two-stage binary counter is shown in which diode AND circuits are used for coupling from flip-flop to flip-flop. Also shown is a faster counter employing carry look-ahead circuits to avoid the long delay required to ripple through all flip-flops in the counter. A block diagram of a shifting register is also shown. The last paragraph of this section discusses the inherent delay that is required in a self-gated flip-flop. A delay circuit is illustrated, and a self-gated DCTL flip-flop is shown.

The second section of Part 7 illustrates eighteen different logic circuits. Included are seven counter circuits, two shifting registers, two half adder circuits and two exclusive OR circuits. Also illustrated are a TRL block, a diode-transistor block, a diode-transistor matrix, and two current switching circuits.

Parts 6 and 7 of this book illustrate the different types of switching circuits that are used today. A considerable number of different circuits are represented and this information could be of value to people who require specific circuits for experimental work and do not care or do not have the time to design them. There is very little information given on the operational characteristics of the circuits. The sections on design procedures are short, and an inexperienced circuit designer will find them rough going. In the section on DCTL design, nothing much was said about the problem of base robbing which occurs when parallel loads are driven. Also the advantages silicon transistors offer in an increased on, off voltage margin are not discussed.

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Integrated Magnetic Circuits for Synchronous Sequential Logic Machines—U. F. Gianola. (*Bell Sys. Tech. J.*, vol. 39, pp. 295–332; March, 1960.)

Since the publication of Wang and Woo's paper, "Static Magnetic Storage and Delay Line," ten years ago, much effort and sophistication have gone into the development of magnetic logic circuits without employing other nonlinear components. The shift-register type of circuits for synchronous sequential logic showed good promise. The recent trend of emphasis on integrated circuits attracted new interest to such circuits.

Gianola's paper is a significant contribution to this field. It is an excellent tutorial introduction and clearly spells out the pertinent properties, requirements, and limitations of core (single- and multi-aperture) logic circuits. The examples given in Section IV serve well to illustrate the ways and means of obtaining gain and providing unilateral transmission of signal in those circuits. The brief analysis included in the appendix provides a quantitative picture of operational conditions, as well as limitations on fan-out and operation speed.

The section on sheet logic contains fresh and interesting observations and deductions. Some of the items are in the category of "interesting and reasonably practical possibilities," as expressed by the author. Although practical, high-speed, fully integrated magnetic systems are not in sight, this reviewer shares the author's enthusiasm for future development in this area.

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Negative-Resistance Elements as Digital Computer Components—Morton H. Lewin. (*Proc. EJCC*, pp. 15–27; December 1–3, 1959.)

In the first three pages of this paper an attempt was made to present a generalized discussion on the use of two-terminal negative resistance devices as digital computer components. Since a tw terminal negative-resistance device, in general, may have a mu more complex characteristic in nature than that of a tunnel diod it becomes obvious that it was not the author's intention to discu either the properties or the possible applications of a negative-resis ance element in general. Consequently it appears that the first thr pages served only as an introduction on a grand scale for this pape Perhaps a more appropriate title for this paper might be "Tunn Diodes As Digital Computer Components."

The qualitative description of various tunnel diode circuits suc as threshold gates and inverters are adequate for the purpose of i troducing a new device and some of its possible modes of operatio

In the paragraph under the title of unilateralization, the discu sion is too brief for such an important subject. In the example whe the inverter circuit or a threshold gate is driven by an elevated ou put, the presentation is so brief that it might lead one to believe m takenly that this technique is applicable in a general form and is effective as the use of common rectifying diodes (or backward diode or the three-phase supply scheme for the "Goto-pair."

In the conclusion, the statement that the experimental resul demonstrated reliable operation seems somewhat hasty. Since figures of tolerance of components were given, and according to t paper all the currents from the power supply were adjusted for prop operation during the experiments, the definition of reliability is n clear here.

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[2] W. F. Chow, "Tunnel Diode Digital Circuitry," presented at 1960 Interna Solid-State Circuits Conf., Philadelphia, Pa., February 10–12, 1960; also IR Trans. on Electronic Computers, vol. EC-9, pp. 295–301; September, 19

On Microelectronic Components, Interconnections, and Syste Fabrication—Kenneth R. Shoulders. (*Proc. WJCC*, pp. 251–25 May 3–5, 1960.)

This paper can best be considered as a thought-provoking vis with an enthusiastic and imaginative colleague. It contains a val able collection of ideas, suggestions and some wishful thinking abo micro-computers. Except in passing, it neither reports nor claims report details of existing experimental accomplishments. If the su gestion of a computer occupying one cubic inch and having 10^{11} activ components tempts you to smile and pass on, don't. The author basic objective is to suggest an answer to the question, "What kin of micro-computer technology should be ultimately practical wit electronics?" instead of to the more usual question, "What is th best incremental advance from present techniques and devices?"

The ultimate device suggested combines thin film and vacuu tube technology with a field-emission vacuum tetrode one micro square composed entirely of two refractory materials deposited o a passive substrate. Because of its small size most of the usual ob jections to field-emission electron devices are replaced by difficulti in fabrication. The paper includes, however, discussion of an electro or ion-beam machining technique that seems to hold great promi for integrated circuitry. The field-emission tetrode depends on th high fields around micro-points which eventually might be sel formed by the micro-machining techniques mentioned above. Re ability and stability are enhanced by use of only two materials (a r fractory metal and a dielectric), by vacuum encapsulation, and b super-cleanliness in processing. No completed device of this kin exists but all the principles have been demonstrated, including tho of micro-machining.

Although the paper is clearly device-oriented, the author h some intriguing notions for circuit and systems people on the o hand and for materials people on the other. Among the ideas di cussed from the systems and equipment standpoint are the combin tion in one computer of complexity approaching that of the huma neural system with speed of modern electronic technlogy and wi portability. Another idea is the proposal to have connection modul tion by which the computer determines and carries out much of own wiring after the components are installed.

For the circuit and interconnection man the ideas range from ectronic fabrication of circuits through electron beams and optical upling using wide-band serial techniques down to an auxiliary mputer to handle internal communications on a sampled-data asis. The author makes the interesting assumption that the connec-ons associated with each active device in a practical micro-com-ıter will require three times the volume of the active device, *i.e.*, ree square microns multiplied by the combined device and sub-rate thickness.

A novel definition of a perfectly reliable device as one in which ne of the material composing it is allowed to move or migrate ads to interesting speculations for the materials man. Among the eas discussed are the reactive depositions of two materials, a single nductıng material and a single insulator, from which the entire rcuit and system are built. The advantages of high temperature eactions in high vacuum, and the nonavalanching bonus in dielec-ric strength enjoyed by submicron thin films of dielectrics, are also iscussed.

Although the organization and style of the paper are not always ntirely clear, and though many may challenge some of his assump-ons, the author has successfully unfettered his imagination and imulated ours.

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Chemical Switches—B. K. Green, E. Berman, B. Katchen, L. chleicher, and J. J. Stansbrey. (*Proc. Internatl. Symp. on Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Lab-ratory," Harvard University Press, Cambridge, Mass., pp. 316–325; 959.

This paper deals with the use of photochromic chemical material s switching devices. Two stable states (one colored and the other olorless) may be achieved by imposing a particular wavelength of ght on the chemical material, ultraviolet light yielding a blue color nd yellow light removing the color. Unfortunately, the major part f this paper deals with the chemical aspects of the particular photo-hromic material under investigation and contains only a brief quali-ative discussion dealing with the switching or storage features. Along his line details are presented on very interesting laboratory experi-ients involved in forming membrane material and on the selectivity f these membranes.

Mention is made of the storage capacity of fabricated cells of hotochromic material, the possibility of read-write cycles and the tability of the device, but only in a very brief and passing fashion. No comments are made regarding the fact that a switch of this type nust have a short time constant and must be absolutely reliable. A urther unanswered question which the authors do not discuss is vhether the two stable states of color vs no color are actually chieved. In other words, does the yellow color actually produce a olorless state in the true sense or only approximate it?

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Memories

Characteristics of a Multiple Magnetic Plane Thin Film Memory Device—K. D. Broadbent, S. Shohara, and G. Wolfe. (*Proc. WJCC*, pp. 97–103; May 3–5, 1960.)

Magnetic film devices are growing in both number and complexity as illustrated by this paper. It describes a multilayer magnetic film memory device which utilizes the magnetic field associated with the divergence of the magnetization to achieve preferential arrangements of the magnetization vectors.

This memory element operates on the same magneto-static energy principle as the multiaperture ferrite core[1,2] devices and represents a magnetic film embodiment of the ferrite-type device.

The greatest significance of the paper lies in showing, apparently, that multilayers of magnetic, insulating, and conducting materials can be fabricated satisfactorily; such techniques are necessary to obtain optimum performance and miniaturization from film devices.

Unfortunately, the authors were extremely sketchy in reporting information about the materials used, the procedures employed, and the results obtained. By calculating from the little data given, it is possible to get estimates of film and insulation properties and size.

However, the scientific value of this paper has been considerably reduced because of the lack of this information.

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A Tunnel-Diode Tenth-Microsecond Memory—M. M. Kaufman (1960 IRE International Convention Record, pt. 2, pp. 114–123.)

Tunnel diodes have many useful applications that may establish the device firmly in the semiconductor components area; however, memory applications appear to be the least promising area of tunnel diode use.

The paper presents a clear and obviously honest report of the important considerations required of the tunnel-diode characteristics for proper memory operation. Undoubtedly, their high-speed capabilities appear to offer an advantage in memory applications, but there are important limitations that would seem to prohibit their general use. All memory elements presently in use admittedly leave much to be desired and in fact represent compromises in speed, power, size and cost. Generally, a memory element prospers if in weighing these factors no overwhelming compromise is made. For example, the high current requirements of ferrite cores is offset by their zero standby power requirements. The low output voltage of thin films is offset by their inherent high-speed capabilities. The tunnel diode as reported in this paper has many disadvantages for memory applications with the possible high-speed operation its only redeeming feature.

The paper shows that the tolerances required of the tunnel-diode characteristics for memory use will not permit low cost units, at least not comparable to present memory elements. There appears to be no minimization of driving equipment or other conventional memory circuits that will offset the high element cost. The packing density even with the proposed unique design for the tunnel-diode elements results in a volume per bit that is at least two orders of magnitude greater than present memory elements. This last point gives rise to serious doubts that very high-speed operation can be achieved in a moderate size memory since the large volume per bit requires long drive and sense lines that will contribute to delays and increased memory-cycle time.

The parallel driving design described in this paper imposes large standby power requirements that may reduce margins. Even with the 5 milliwatt per bit maximum specified, a memory of 200,000 bits will dissipate a kilowatt of power and limit the packing density substantially. The packing density must be minimized to achieve high speed but cannot exceed the safe limits of heat transfer from individual elements. Although this standby power is considered by the author, no mention is made of the heat problem of an element that is continually being selected. The problem this imposes on minimum packing is important and must be considered in obtaining a realistic packing density.

The memory design described in the paper places the tunnel diodes in a parallel drive arrangement. Since it is possible to use a series design, some mention might have been made about its comparative value.

The author does demonstrate a general appreciation of memory requirements, and the discussion of the optimum tunnel-diode characteristics relative to the memory requirements is particularly good. For those interested in tunnel-diode memory design it should be a worthwhile guide.

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Unifluxor: A Permanent Memory Element—A. Renard and W. J. Neumann. (*Proc. WJCC*, pp. 91–96; May 3–5, 1960.)

The Unifluxor is an interesting permanent memory element. The technique used to vary the inductive coupling between the input and the output is quite clever. It presents a fresh solution to the problem of how to modulate this coupling.

[1] J. A. Rajchman and A. W. Lo, "The Transfluxor," Proc. IRE, vol. 44, pp. 321–332; March, 1956.
[2] N. F. Lockhart, "Logic by ordered flux changes in multipath ferrite cores," 1958 IRE National Convention Record, pt. 4, pp. 268–278.

As Renard and Neumann state in their opening paragraph, the coupling between input and output may be either linear or nonlinear. Linear coupling may be provided by inductive, capacitive, or resistive techniques. The principal advantage of linear coupling is that, since no thresholds are involved, it is possible to work at any convenient power level. In some applications this can be quite important. The lack of a thresholding characteristic, however, imposes severe restrictions on the access circuits if the array size is at all large. Or, to say it another way, since nearly ideal address-selection switches are required, the cost per bit contributed by the access circuits will be quite high, as pointed out by the authors.

It is stated that one of the important design parameters is the "final amplitude of the current," in that it determines the spacings of the sense and drive strips. It would seem that in a linear system the signal-to-noise ratio would be independent of the drive-current magnitude. In fact, excluding pickup from external sources, this must be so.

The Unifluxor is capable of a rather high speed of operation. This fact, plus the apparent simplicity of fabrication, wide temperature range of operation, and wide range of operating currents should make the Unifluxor a valuable addition to the growing list of permanent memory elements.

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A Word-Oriented Transistor Driven Non-Destructive Readout Memory—T. C. Penn and D. G. Fisher. (*Proc. WJCC*, pp. 83–90; May 3–5, 1960.)

Penn and Fisher describe a transistor-driven nondestructive readout memory using a novel magnetic matrix switch with a three-aperture ferrite memory cell. The authors list a good set of references dealing with the multiaperture devices and admit that their scheme "superficially differs little from previous such schemes either in driving currents or core geometry." Since there are many modes of operating these multiaperture devices, a paper[1] on the flux patterns within these cells is very helpful to those contemplating using them.

If a memory system is large enough and fast enough, the drive lines will assume transmission-line characteristics, making the drive problem quite different from that of a slow system. Drive currents and characteristic impedance of the line determine the back EMF's of a transmission line. If the system is slow and does not take on transmission-line characteristics, the back EMF's will be composed of the sums of the EMF's of each stored bit.

It is questionable whether the system described can be fast enough or large enough to act as a transmission line. If this is the case, the back EMF's presented to the switch core are then composed of the individual back EMF's of each memory core, and will vary depending upon the stored information.

The SET drive current is the most critical current in the system and must work between a minimum and maximum threshold. If too large a "0" could be changed into a "1," and if too small a "1" could be READ as a "0," a suitable current source from a switch core is difficult to maintain because of the problem of the varying EMF's. This will surely restrict the maximum word length for a given matrix switch core.

The large memory drive currents (0.5 to 3.0 ampere turns) required by the three-aperture memory cell are cleverly provided by their magnetic switch matrix. The matrix switch is operated with row and column inputs in a complementary excitation mode, whereby all rows and columns are excited except the row and column of the addressed core. The exciting row and column currents are summed in the addressed core. For an n-squared matrix the currents in the addressed core are $2(n-1)$ times the current of each driver. The particular matrix winding configuration requires a varying number of turns for the row and column windings; in an n-square matrix $2(n-1)$ turns are required per input drive winding.

In an extension of this technique the reset of the switching matrix is produced by using the output from an identical complementary switch matrix. It is proposed that either switch matrix could be used for either function.

This scheme of current summation and reset action is limited i matrix size because of 1) increase in the row and column turns wit increase of matrix size, 2) back EMF voltages of each resetting ro and column driver when used in the proposed reset fashion, an 3) shunt loading due to the large turns-ratio between the reset tur and driver turns of the reset array.

These three problems become more serious as the size of th switching matrix increases. The minimum number of turns on eac core in the proposed 16×16 matrix would be thirty for each drive one for the series-output winding, one for the reset winding, an one for the memory drive line winding.

The switch-core matrix sums currents into the proper output a the expense of having to drive many shuttled cores. With the pro posed 16×16 array resetting another identical 16×16 array, for th one core reset, each driver of the resetting matrix sees somethir like 991 shuttled turns.

The shunt loading caused by the increase in turns ratio betwee the driver and the reset windings of the reset array increases wit matrix size. For an n-square matrix the voltage across the row c column lines (from the bus to the driver) is $2n(n-1)$ times the vol age of one shuttle turn. This voltage would be 480 times one shutt turn for the 16×16 matrix, and although of a polarity to turn off th circuit shown in Fig. 6, could exceed the voltage breakdown of T

It appears then, that the switch matrix is limited in size. Probabl an 8×8 would be practical, but would restrict the size of the memor module constructed by this technique.

Whether or not the over-all system could compete with othe nondestructive memory systems in view of the complex winding pa terns required, and the relatively slow interrogating rates possibl is debatable.

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Programming

Mathematical Methods for Digital Computers—A. Ralston an H. S. Wilf, Eds. (John Wiley and Sons, Inc., New York, N. Y 1960. 293+viii pages.)

This book is a collection of twenty-six chapters by twenty-tw authors—each concerned with one numerical solution process for typical applied mathematics problem. Thus, J. Greenstadt discusse "The Determination of the Characteristic Roots of a Matrix by th Jacobi Method" for nine pages while E. L. Wachspress treats "Th Numerical Solution of Boundary Value Problems" in seven page Among other topics we find linear equations, matrix inversion, ord nary differential equations (initial conditions), parabolic, ellipti and hyperbolic partial differential equations, analysis of varianc multiple regression analysis, roots of polynomials, and linear pro gramming solutions.

Since the book is clearly intended to be an exposition of standar techniques, this reviewer must criticize the publishers for choosin an editor-contributor structure for this volume. Within the limita tions of such a structure, this book is a good job; but the limitation are serious. A strong editorial hand has successfully imposed a stanc ard format on these separate expositions, but the quality of the expo sition is uneven. In the first numerical method discussed, A. Orde describes the solution of simultaneous linear equations by direc methods in a style better suited to a mathematics journal than a expository article on a fundamental elementary subject. At no poin does he explain that he is describing an implementation of the ord nary, high school, eliminate-one-variable-at-a-time technique. He re fers instead to the "classical Gauss-Jordan approach" and his discu sion is couched in terms of matrix products, some of which turn ou to be mental constructs which never appear as stored quantities i the final computer program. This reviewer suggests that a reader wh did not already know how to solve simultaneous equations by direc elimination is probably not going to learn from Mr. Orden. On th other hand, a person who has already programmed direct eliminatio and is familiar with the general concepts will appreciate a number c suggestions for combining several closely related topics into a sing general program and will enjoy the description of a very satisfactor permutation algorithm. By way of contrast, Mary Lister discuss the numerical solution of hyperbolic partial differential equatio by characteristics with a clarity that is unavailable in any other trea ment of this subject. (But she needed 25 pages.)

[1] S. A. Abbas and D. L. Critchlow, "Calculations of flux patterns in ferrite multipath structures," 1958 IRE National Convention Record, pt. 4, pp. 263–267.

Another major difficulty—directly ascribable to the one author, e subject arrangement—is a dearth of discussion comparing and ıtrasting alternative methods for the same type of problem. Thus book presents three methods for matrix inversion, three for the ution of linear equations, and two each for the integration of ordi- y differential equations from initial conditions, elliptic partial dif- ential equations, and hyperbolic partial differential equations. The ative merits might well have been treated by an introductory page each section, presumably by the editors. As the book stands, the der receives little or no guidance. Thus, although the conjugate dient and Gauss-Seidel methods for simultaneous linear equations both adequately presented, their expositors are so intent on tail that they fail to point out the important general property that th these methods are *iterative*—which makes possible the use of *priori* engineering knowledge about the probable nature of the solu- n. Such considerations can be decisive in choosing a computa- nal method, since a good guess can combine with an iterative ethod to produce a saving in computation time which is much eater than anything to be gained by some of the small polishings at are possible in direct techniques.

The first chapter is an exception to the general format. It contains rather sophisticated discussion by E. G. Kogbetliantz of efficient proximations to the standard engineering functions. The uninitiated will find it rough going, but worthwhile.

On the positive side, this book is a useful compendium of computational information handily collected into one volume. Currently it s no competitors. This reviewer's objections stem principally from ıs of omission which are a concomitant of its method of construction. If we accept each author's scope and the expositional level he s set for himself, then objections vanish. The choice of topics is od (although one might expect that matrix eigenvectors would ırrant treatment by more than merely the Jacobi method). The rmat of a mathematical discussion followed by heavily annotated w-charts and a sample problem is also good. Estimations of emory requirements and running times are certainly helpful and references to the pertinent literature at the end of each chapter e exceedingly useful. The printers have done a good job with difult material (the only typo this reviewer noticed was $\bar{y}$ where y' ıs intended on page 128). Considering the diversity of the sources, e homogeneity of presentational style bespeaks both firmness and gilance in the editorial staff.

In summary: it is good, though it might have been better; it is t apt to be supplanted soon.

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ıe Generation of Pseudo-Random Numbers on Electronic Digital ɔmputers—A. R. Edmonds. (*Computer J.*, vol. 2, pp. 181–184; nuary, 1960.)

The author considers the family of sequences $u_0, u_1, \cdots$ of ıst positive residues modulo a positive integer m: $u_0=a$, $u_1=ka$, $=k^2a, \cdots$, where a and k are preassigned numbers, each relarely prime to m.

He states that a program, Pegasus library routine R980, has en written for the Ferranti Pegasus for the choice of parameters $=2^{31}-1$ and $k\equiv 13^{13}$. The choice of a is immaterial here, since k is primitive element in the multiplicative group of positive residues ɔdulo the prime m, and hence choice of a different a merely causes e to enter at different points in the cycle 1, k, $k^2, \cdots, k^{2^{31}-3}$. ests of very long samples of the output have shown it to fulfill "for ɔst practical purposes" certain criteria of randomness. He states rther that a similar program has been written for the Ferranti Merry using different values of the parameters, and that results of sts being conducted on the sequences produced will be reported bsequently.

It seems to the reviewer that studies of the type announced in the ticle under review are of definite value in providing high-rate urces of pseudo-random numbers together with a catalogue of their mbinatorial properties.

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Analog Computer Systems

An Analog Computer Nyquist Plotter—E. A. Goldberg. (1960 IRE International Convention Record, pt. 2, pp. 41–46.)

The automatic Nyquist plotter appears to be a convenient way to plot Nyquist diagrams of laboratory simulations in a noise-free environment. One could get the magnitude and phase of any transfer function by this process:

The greatest weakness in the procedure presented arises from its sensitivity to noise or waveform distortion. Anyone who has tried to repeat measurements on mechanical equipment with stiction and some backlash will be skeptical of relying on the pair of single-point samples of the output used to obtain the transfer function. Much more meaningful measurements can be obtained by feeding the signal $\epsilon(t)$ through an amplifier and phase shifter and subtracting the signal thus obtained from the output. The amplifier gain and phase are adjusted so as to obtain a null of the difference. When the null is obtained, the amplifier gain and phase are the magnitude and angle of $F(s)$. The sort of null detector thus used determines the nature of the approximation made to measuring $F(s)$.

The use of the automatic plotting technique on a sampled-data control system is particularly bad because the sampler introduces sampling ripple which makes both the output and error signals nonsinusoidal. Almost all measurements tied to samples of the output at zero crossings of the error and its phase-shifted component will clearly be in error. If the sampling frequency and the signal frequency are not commensurate, the whole system excitation will not actually be periodic, and the patterns described by the author occur. It should be noted, however, that in many practical cases the variation in the zero crossings of $\epsilon(t)$ may be so great as to obscure the meaning of the measurements made automatically.

The practical worth of the automatic Nyquist plotter depends upon the balance between its convenience in automatically plotting a transfer locus and its weakness due to its sensitivity to noise. I fear that its weaknesses greatly overshadow its conveniences in many practical cases.

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An On-Line Solid-State Analog Computer for Automatic Gas Flow Compensation—F. P. Simmons. (1960 IRE International Convention Record, pt. 2, pp. 96–108.)

Mr. Simmons' paper has attempted to cover a bit more than its title would indicate, and has suffered in its clarity as a consequence. Basically, three separate topics are covered in this paper. First, a rather protracted discussion of several forms of empirical equations which relate the flow of gas, reduced to standard conditions, through an orifice plate to the temperature, pressure, specific gravity, and pressure drop of the gas; secondly, an analysis of the errors which are committed in a manual system which operates from chart recordings of these variables, and thirdly, a high-precision analog computer is described, and the results of some tests are given.

To cover these topics in order, the discussion of the empirical equations serves a very useful purpose, in that the reader is made aware of the fact that even the simple problem of metering gas flow, simple as it is in comparison to the usual problems of industrial chemical instrumentation involving multicomponent and multiphase polymers and slurries in distillation columns, reactors, etc., is a far cry from nice, well-behaved and understood electron and radiation flow, both qualitatively and quantitatively. Although no standard fluid mechanics reference is cited in the paper, the empirical relation between flow and measured parameters used is the following:

$$Q_h = K\frac{(h_w P_f)^{1/2}}{(T_f G)^{1/2}},$$

where h_w is the pressure drop across the orifice plate; P_f is the static pressure of the gas; T_f is the absolute temperature of the gas; G is the specific gravity of the flowing gas; and K or Discharge Coefficient is a proportionality factor determined from viscosity, Reynolds number, etc. Forms of this empirical equation differ in that temperature and specific gravity may or may not be incorporated into the "constant" K, and the author shows that these differing forms result in a spread of 2 per cent in the volumetric flow Q_h that was computed

for a specific example. Since Simmons was attempting to describe a computer to be used with orifice plate flow measurement, a comparison with the inherent accuracy of other techniques such as venturi, or more recent mass flow measuring devices was not mandatory, but would have been helpful to the reader, since higher accuracies are possible, even if not economically justified.

The second part of the paper which deals with the errors made in manually integrating circular chart recordings of the parameters by polar planimeter is quite complete, but neglects the consideration of other methods, such as a digital computation scheme. This section also justifies inclusion of specific gravity as a constant rather than a parameter, on the ground that normal variation of G in a pipeline is on the order of 1 per cent, which is of the same order of magnitude as the error in its measurement. Both of these assumptions might be open to question.

The third section of the paper deals with a computer which solves an equation of the form

$$Q_h = \sqrt{\frac{KP_fH_w}{T_f}}$$

where the parameters are in the form of voltages fed to the computer, and the K is a potentiometer setting. The author shows an error analysis which gives an accuracy of 0.5 per cent to the computer itself, assuming perfect measurements, as well as a table of experimental results which show even higher accuracy. Several minor criticisms can be made with respect to terminology, such as "dynamic range" and "bandwidth" which the author uses in an amplitude rather than time or frequency sense. In addition, although a reference was given, a more detailed explanation of the computer circuitry would have proved helpful in determining the validity of accuracy claims, etc.

Since the author is only passingly interested in the general usefulness of such a computer, and is most concerned with establishing its usefulness as a device for actually measuring natural gas flow through orifice plate instrumented pipelines, then his device can only be judged as a part of the measuring system for such an application. In such a case, laboratory standards and criteria must be replaced by considerations that realistically can represent usage, unattended, in a remote station. Little mention is made of the inherent accuracy of the basic measuring transducers for pressure and temperature, and their noise, drift, range, etc.

If these have an accuracy which is appreciably less than the computer, then high accuracies on the part of the computer will not appreciably affect the over-all measuring system. As far as the computer itself is concerned, no mention is made as to its inherent drift, or the effect of noisy measurements, or of the accuracy of its power requirements, or of its reliability, although all of these have presumably been considered by the author.

In summary, this paper, while representing a contribution to the art of gas flow measurement, does not present a completely objective view of this or alternative methods of making such measurements, with or without digital or analog computers.

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"Anatran"—First Step in Breeding the "Diginalog"—L. A. Ohling (*Proc. WJCC*, pp. 315–328; May 3–5, 1960.)

Allegory comes to the computer field—in the form of a br description of a hypothetical three-act play starring Don Digital a Ann Analog. Eschewing the language barriers and traditional d crimination between clans, the author describes the inevitable cou ship, engagement, and marriage and predicts as progeny a new cla of "machina sapiens"—the "Diginalog." Beneath the heavy coati of metaphor in the play and in the latter two-thirds of this paper found a description of "Anatran"—a problem-oriented language f digital-to-analog computer communication (so necessary to t "courtship")—developed in the author's computing center where i tegration of analog and digital techniques and computers is emph sized. Reference is made to the "engagement" of digital and anal by means of present-day automatic pot setting equipment (digital controlled). "Union" of the two is only briefly discussed in terms direct digital control of an analog computer, a combination of exis ing systems "exploiting the best features of each." A few suggestio are made relating to the features and philosophy of the Diginalc that "paragon" of computer accomplishment.

Anatran is a digital computer program for translating from problem-oriented statement of a mathematical problem, which is be programmed for an analog computer, to a wiring flow diagram, list of potentiometer settings, and a count of the required anal computer components. Anatran is illustrated for a typical proble (longitudinal motion of an aircraft with control by an autopilo with illustrations of analog flow diagrams prepared both by machi and by hand. This method of programming an analog computer wi a special digital computer program appears to be well conceived a most probably will produce useful results in the reduction of huma errors and programming time.

In this writer's opinion, the Anatran approach should be mc interesting to the large computer laboratories that may be short really experienced analog computer programmers. This observati is made without any desire to obstruct progress but rather in reco nition of the limitations and vagaries of analog components. T "best use" of particular components, the "best" component for a pa ticular function, and the anticipation of "difficult" circuit configur tions are subjective matters which support the belief that there is bit of "art" in good analog programming. A review of the Anatr analog program by a human expert is recommended until Anatr has been augmented to accommodate a full description of the cha acteristics of every analog component under varying circumstanc Such a review should not detract from the usefulness of Anatran.

Although not brought out in the example problem it is assum here that Anatran is capable of complete magnitude and time scali of all analog components. If this is not so, the usefulness of the pr gram must be questioned seriously.

For the most part the new ideas presented in this paper are spec lative and intentionally tentative. One would have appreciated fuller description of the author's conception of the Diginalog, mo supporting arguments for his projections, and some compariso with alternative approaches which he probably has evaluated.

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Abstracts of Current Computer Literature

(THROUGH JULY, 1960)

These abstracts and the associated subject and author indexes were prepared on a commercial basis under the direction of Dr. Geoffrey Knight, Jr., of Cambridge Communications, Inc., 238 Main St., Cambridge 42, Mass.

Additional copies of these abstracts are available from IRE Headquarters, 1 East 79th St., New York 21, N. Y., at $1.00 per copy, or $3.50 for the set of four to be published in 1960.

—*The Editor.*

A-2: EQUIPMENT—COMPONENTS AND CIRCUITS

998

The State of Computer Circuits Containing Memory Elements, A. Van Wijngaarden (Amsterdam, The Netherlands); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 213–224; 1959.

The behavior of digital switching circuits containing memory elements is investigated. The circuits considered include the one digit delay line, coders and decoders, complete feed back circuits, and nonlinear and multiple output devices. Mathematical relations connecting the various parameters are proposed as models to assist the design of such circuits.

999

Microwave Logic, W. D. Lewis (Bell Telephone Labs.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 334–342; 1959.

Three ways of implementing combinational logic based on microwave techniques, namely detection followed by modulation, frequency conversion, and sequential logic in which the basic pulse rate is higher than the reciprocal of the delay in closed loops, are discussed. Basic circuits for AND, OR and NOT functions for each technique are presented. Pulse rates of 160 Mc are claimed to be feasible using the techniques described.

1000

A New Class of Switching Devices and Logic Elements, P. R. McIsaac (Cornell University) and I. Itzkan (Sperry Gyroscope Co.); PROC. IRE, vol. 48, pp. 1264–1271; July, 1960.

A new class of switching devices employing microwave tube elements, whereby appropriate combinations of particular components can create a variety of devices that are capable of performing switching and logic at extremely high speeds (one operation per μsec or less), is discussed. Such speeds represent a large step forward in the computer art. A preliminary device which demonstrates the ability of a microwave signal to control a dc current is described. The goal of operating a computer with pulse trains dictated a choice of components that would provide large bandwidth with gain; therefore, an experimental traveling-wave interaction type tube was built which demonstrated the ability of one microwave signal to control another.

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1001

Solid-State Microwave High Speed Computers, J. A. Rajchman (RCA Labs.); *Proc. EJCC*, pp. 38–47; December 1–3, 1959.

The use of variable capacitance diodes (in parametric subharmonic phase locked oscillators) or tunnel diodes and microwave transmission line techniques in high-speed computer logic and memory circuits is discussed and experimental circuits utilizing these devices and techniques are described. The fabrication of the microencapsulated devices required for these applications is discussed. It is predicted that tunnel diode logic circuits which can operate at 1000 Mc and tunnel diode random-access memories with cycle times of 10^{-8} second can be constructed.

1002

Millimicrosecond Pulse Instrumentation for Microwave, J. T. Tippett (Dept. of Defense); IRE TRANS. ON INSTRUMENTATION, vol. I–9, pp. 32–34; June, 1960.

Instrumentation for application of microwave energy to computer circuits requires that performance of microwave pulse circuits with transition times of less than 0.5 millimicrosecond be easily examined. A circuit utilizing a fast microwave diode switch as an ultrafast rise time pulse generator, a dual output detector, and a traveling-wave oscilloscope for use with pulse amplitude modulated microwave computer components are discussed. Using this same equipment with system modifications, test equipment can be built for phase pulse modulated microwave circuits. The microwave diode switch consists of a special germanium diode mounted in waveguide. Both the diode and waveguide mount were designed for minimum transition time between the operating states of the circuit involved. The detector was designed for use with a 1N23-type diode and has dual coaxial cable outputs. This system, together with a traveling-wave amplifier, was used for displaying pulse power levels of 0.1 milliwatt with easy visual observations on the oscilloscope. No limitations were seen which would prevent this system from being used with lower pulse power levels if a higher-gain low-noise traveling-wave amplifier were used.

1003

Back-Transient Diode Logic, G. Wolff (Polytechnic Inst. of Brooklyn); *Commun. and Electronics* (*Trans. AIEE*, vol. 79, pt. I), no. 47, pp. 4–9; March, 1960.

A method of utilizing the high-current transient which is present when a diode is switched off to improve the efficiency of high-speed logical systems is presented. The back transient, which is caused by hole storage, may be used in systems which exhibit good efficiency, low noise, and compatibility with tube or transistor circuits. Quiescent power dissipation is considerably reduced and is not dependent on switching speed. Low-priced diodes have been used in experimental circuits at clock frequencies up to 30 Mc; sample circuits and waveforms are included.

1004

Esake Diode High-Speed Logical Circui E. Goto, K. Murata, K. Nakazaw K. Nakagawa, T. Moto-oka, Y. Matsuok Y. Ishibashi, H. Ishida, T. Soma, a E. Wada (University of Tokyo); IRE TRA ON ELECTRONIC COMPUTERS, vol. EC-9, p 25–29; March, 1960.

Logical circuits using Esaki diodes whi are based on a principle similar to pa metron (subharmonic oscillator element) c cuits are described. Two diodes are used series to form a basic element called a tw and a binary digit is represented by t polarity of the potential induced at the m dle point of the twin, which is controlled the majority of input signals applied to t middle point. Unilateral transmission of formation in circuits consisting of cascad twins is achieved by dividing the twins ir three groups and by energizing each gro one after another in a cyclic manner. Expe mental results with the clock frequency high as 30 Mc are reported. Also, a del line dynamic memory and a nondestructi memory in matrix form are discussed.

1005

The Design of Diode-Transistor NOR C cuits, D. P. Masher (Stanford Res. Inst IRE TRANS. ON ELECTRONIC COMPUTE vol. EC-9, pp. 15–24; March, 1960.

Considerations leading to the adoption diode-transistor NOR circuitry for a mod ately fast data-processing system are o lined. The design of the basic circuit treated in detail. Development of a uniq set of compatible logic packages from t basic circuit is described. This set is uniq in the sense that a single type of dio transistor circuit is used to provide the gr majority of logic and storage functions quired in the system. This single circuit ty which functions as a NOR circuit, is e bodied in two package types. One packa provides a single gate with a fan-in of fi The other package provides two gates, ea with a fan-in of two. The latter type may externally connected to provide a set-re flip flop. Only two other package types a used. The first is a passive transfer circ which greatly simplifies shift register log and the second is a delay package which closely related to the basic NOR circuit.

1006

A New Method of Designing Low-Lev High-Speed Semiconductor Logic Circui W. B. Cagle and W. H. Chen (Bell Te phone Labs.); *Annals of the Computat Laboratory*, Harvard University Press, Ca bridge, Mass., vol. 30, pp. 161–170; 19

A type of transistor-diode design, t basic gate of which is a diode AND g with a transistor inverting amplifier, is p sented. It has many of the features Direct-Coupled Transistor Logic, while ing far fewer diodes and not requiring special characteristics necessary for DC operation. The circuits utilize distribu gain with small voltage swings at low i pedances, and are capable of supplying la reverse base currents from the transistors. these respects they are very suitable for hi speed logic.

007
ansistor Applications in a High-Speed rallel Computer, J. Connett and P. oke (Metropolitan-Vickers Electrical Co.) *oc. IEE*, vol. 106, pt. B, suppl. no. 18, 1226–1234, 1289–1291; May, 1959.

The use of transistors with diode logic to iisfy some fundamental requirements culiar to binary amplifiers and two-state ments in parallel digital computers is dis- ssed. Feedback saturation control is gen- lly adopted; building-block circuits in- rporating this feature are described. Satis- tory operation at 1 megapulse/sec is ob- ned using 5-Mc alloy-junction transis- rs. Some specific arithmetic and counting plications are discussed. When binary plifiers fail to give adequate frequency ponse or power-handling capacity be- use of transistor limitations, master-pulse hniques may provide a solution. These hniques are discussed and their applica- n to the ferrite-core-store drive problem is scribed.

008
e Use of Multipurpose Logical Devices, Dunham and J. North (IBM Corp.); *nals of the Computation Laboratory*, rvard University Press, Cambridge, ass., vol. 30, pp. 192–200; 1959.

Multipurpose logical elements, *i.e.*, cir- its capable of economically realizing func- ns of three, four, and five variables, are cussed. It is shown that not more than ir full adders made from a two-collector nsistor suffice to realize any function of ree variables. More efficient devices are esented and the efficiency of various four- riable single and multiple-output multi- rpose devices is assessed.

009
rcuit Considerations and Logical Design ith Direct-Coupled Transistor Logic, R. A. udlich (Bell Telephone Labs.); *Annals the Computation Laboratory*, Harvard Uni- rsity Press, Cambridge, Mass., vol. 30, . 201–210; 1959.

The basic principles of Direct-Coupled ransistor Logic are summarized and the use DCTL circuits as the basic building blocks the TRADIC Leprechaun Computer is scribed. The influence which component lvantages and limitations have on logical sign is assessed, and a plea for closer inte- ation of the functions of logical and circuit sign is made.

010
vestigation of High-Frequency Transistor gic Circuit for Digital Application, Wong (Naval Ordnance Test Station); *S. Govt. Res. Repts*, vol. 33, p. 535 (A), ay 13, 1960; PB 145 166 (order from LC i$5.70, Ph$16.80).

The design of a logic module employing nction transistors is discussed. This pack- e, which is designed as a standard module r logical operation in a digital computer, nploys NOR logic in place of the usual ND, OR, and NOT functions. The inciple of threshold operation for the OR circuit is introduced; this character- ic increases the versatility of the logical eration. The worst-case design philosophy s been employed in the design technique. The circuit analysis of this module includes the various input and output loading conditions. A small-signal equivalent circuit for saturation operation is also presented.

1011
Transistor Storage and Logic Circuits for Binary Data Processing, R. Herman (Plessey Co.); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 663–674, 698–701; May, 1959.

Transistor storage circuits for binary data processing in which the active state is defined by the generation of a pulse waveform across the output windings of a transformer and the timing of the output signal is controlled by a clock waveform coupled to each circuit are described. Logic circuits can be designed in which the output voltages generated by different storage circuits are combined additively or subtractively by series connection of a group of output windings. The inclusion of a diode in each series-connected group allows parallel connection of several groups, so that logic circuits corresponding to complex logical functions may by constructed with diodes as the only components. Any of these logic circuits may be made to control the state of an associated storage circuit (delayed or undelayed) by direct connection of the output terminal of the logic circuit to the input terminal of the storage circuit. A design for a parallel adder in which undelayed storage circuits are used for the "carry" register and in which the addition process is completed in a single clock cycle is given.

1012
Transistor Circuits for a Digital Differential Analyzer, G. C. Rowley (A. V. Roe and Co., Ltd.); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 685–687, 698–701; May, 1959.

A two-stage storage circuit, an OR gate, an AND gate, and a binary adder which utilize a half-digit delay circuit are described. The basic circuit includes a junction transistor, two point-contact diodes, a resistor, and a capacitor. The capacitor is the storage element and can be discharged through the transistor and recharged from the applied clock waveforms through one of the diodes. The binary digits 0 and 1 are represented by a fully charged capacitor and a discharged capacitor, respectively. The circuits have been tested in a prototype digital differential analyzer, and it has been found that reliable circuits can be constructed.

1013
High-Speed Digital Computer Circuits Using Transistors as Bidirectional Switches, G. Ord and P. L. Lewis (Royal Radar Establishment); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 828–833; May, 1959.

Circuits which use transistors as bidirectional switches in conjunction with bistable circuits and short delay lines are discussed. The bistable circuit is of a type from which registers used in a digital computer may be assembled. By connecting bidirectional switches in various ways between digits of registers, any one of the operations of transfer, exchange, shift, and count can be carried out in a time less than 0.2 μsec. The transistors used in the bistable circuit and for bidirectional switches are of the surface-barrier type. The delay cable provides a delay of 60 μsec.

1014
Transistors in Combinational Switching Circuits, S. H. Caldwell (Mass. Inst. Tech.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 139–143; 1959.

The switching properties of transistors in simple configurations are surveyed, and similarities and comparisons with other switching elements are developed. The degree to which a transistor may be considered a bilateral and a current steering device, and hence used to replace relays in contact networks, is critically discussed.

1015
A Transistor DC Amplifier for Use in Analogue Computers, C. M. Cundall, J. K. Saggerson, and G. Shaw (Ferranti Ltd.); *Proc. IEE*, vol. 106, pt. B, suppl. no. 18, pp. 1354–1364, 1394–1398; May, 1959.

The use of transistors in place of thermionic valves and electromechanical relays in dc amplifiers for analog computers, as a potential means of reducing their size and power consumption and of increasing their reliability, is discussed. The transistor operational amplifier is analyzed when used as a summing amplifier and as an integrator, thus specifying the characteristics required to give a computing accuracy of better than 0.1 per cent per stage in conventional real-time analog computers. The amplifier designed to meet these requirements is in two parts, both of which are described. An analysis of the resulting double-loop amplifier enables the principal parameters to be chosen to maintain a stable system with the necessary gain over the range of operating frequencies. Test results obtained on a printed circuit version of the amplifier show its performance to be adequate for the majority of analog computing applications.

1016
Transistorized Central Pulse Generator for Digital Equipment, D. J. Grover and J. M. C. Dukes (Standard Telephones and Cables); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 824–827; May, 1959.

An automatic method of maintaining synchronism between the different timing waveforms produced by a central pulse-generating equipment in any large-scale digital equipment, such as a computer, is described. Certain problems arise in the design of these systems, principally because of the limited power output of transistors and their relatively slower switching speeds compared with hard valves. In the servocontrol system described, the output waveforms are examined and compared; and correction signals that control variable-delay devices inserted in the appropriate amplifier chains are generated.

1017
Analysis of Magnetic-Amplifier Circuits, T. H. Bonn (Remington Rand Corp.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 149–160; 1959.

Magnetic amplifier and transistor logical circuits are compared, and it is concluded that the only serious disadvantage of the magnetic circuitry is the inherent delay associated with the magnetic amplifier. The basic magnetic amplifier circuits are catalogued and means for reducing delay are discussed. Coil gating circuits competitive with transistor circuits are presented and an analogy with relay networks is drawn.

1018
Transistor Circuits for a Ferrite Store, G. C. Padwick and A. L. Cain (Mullard Radio Valve Co.); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 675–684, 698–701; May, 1959.

Transistorized circuits associated with a coincident-current ferrite store are described. A switched-current pulse generator which supplies the drive pulses to the store makes use of the high-frequency power transistor type 0C23. Selection is done economically by using gating matrices controlled by transistors. Junction diodes type 0A10, or gold-bonded point-contact diodes type 0A5, pass the current pulses in the matrices with a very small voltage drop. Two methods of gate selection and drive are described, one using square-hysteresis-loop cores to select and drive the gating transistors, and the other using a diode matrix to provide potential levels at the bases of the gating transistors. The output of the store is amplified by high-frequency transistors, strobed, and standardized. Provision is made for writing new information, or for rewriting information immediately after it has been read by a diode logical network controlling the "inhibit" pulse generator.

1019
Flux Reversal in Soft Ferromagnetics, E. M. Gyorgy (Bell Telephone Labs.); *J. Appl. Phys.*, suppl. to vol. 31, pp. 110S-117S; May, 1960.

Many aspects of flux reversal in soft ferromagnetic materials may be interpreted in terms of three types of flux reversal processes. These three types are domain wall motion, nonuniform rotation, and uniform rotation. It has been shown that in general wall motion is the predominant mechanism for values of the applied magnetic field slightly in excess of the coercive field, that nonuniform rotation predominates for intermediate magnetic fields, and that uniform rotation predominates for large fields. The salient features of these three types of flux reversal are discussed and compared with experimental findings. Special emphasis is given to polycrystalline, square-looped ferrites and thin Permalloy films. The importance of geometric effects is illustrated in a review of detailed models for the uniform and nonuniform rotational processes. Specific limitations of the existing models are discussed, and possibilities for future advances are briefly outlined.

1020
Ferrite Films—New Logic and Storage Devices, J. M. Brownlow, W. L. Shevel, Jr., and O. A. Gutwin (IBM Res. Lab.); *J. Appl. Phys.*, suppl. to vol. 31, pp. 121S-122S; May, 1960.

The fabrication of magnetic devices for storage and switching applications in digital computers in the form of open flux path elements is described. The geometry employed is that of a planar film with thicknesses in the range of 5 to 50μ and other dimensions in the fractional inch range. These elements have the advantages of a ferrite composition and of open flux paths without many of the disadvantages present in similar metallic devices. For use in storage systems, these devices possess excellent squareness characteristics and have coincident selection times comparable with ferrite-toroidal devices. Properties of these devices are given in terms of switching curves, low-frequency hysteresis loops, and one-to-zero signal ratios. Other aspects that are discussed include disturb sensitivity of storage elements, heating effects due to high pulse repetition frequency and mechanical properties. For each of these, comparison is made with other types of magnetic elements such as toroids and metallic films. Applications are discussed in terms of drive requirements, packing densities, and switching times.

1021
Specifying a Pulse Transformer for Computer Use, R. R. Blessing (IBM Corp.); *Commun. and Electronics* (*Trans. AIEE*, vol. 79, pt. I), no. 47, pp. 44–47; March, 1960.

The critical requirements of current-driven pulse transformers used as inputs to large-scale ferrite core memories and as switching devices in computer logic are discussed. It is shown how the transformer specifications are arrived at, how the devices are measured, and how these characteristics are related to the application.

1022
Studies in Partial Switching of Ferrite Cores, R. H. Tancrell and R. E. McMahon (M.I.T. Lincoln Lab.); *J. Appl. Phys.*, vol. 31, pp. 762–771; May, 1960.

The characteristics of Mg-Mn ferrite cores in a partially switched state are investigated. Questions relating to the percentage of flux switched at various locations within a core, as well as the speed of this switching are considered. Results show that the amplitude and duration of the set pulse has a pronounced effect on the core behavior. It has been found that most of the variation of the switching waveform among different regions is due to the geometry of the core. Models to describe the experimentally-observed behavior are proposed. The operation of partially switched cores in a fast memory and the investigation of various memory schemes are discussed. Possible applications of the partially switched cores to digital computers are mentioned.

1023
Effect of Previous History on Switching Rate in Ferrites, R. W. McKay and K. C. Smith (University of Toronto); *J. Appl. Phys.*, suppl. to vol. 31, pp. 133S-134S; May, 1960.

Existing theories of switching of square-loop ferrites indicate that the rate of switching is a function of the present state of magnetization of the applied field. Experiments which show that the switching rate is also dependent on previous history are describ
Two cases have been studied. In the f
case, the ferrite was partially switched t
predetermined extent by a pulse of varia
amplitude and then the switching cycle
completed by a pulse of fixed amplitude.
the second, the ferrite was brought to
remanent state by a pulse of variable am
tude before the switching cycle. Changes
great as two to one in switching rate w
produced by variations of previous tre
ment.

1024
Fast Switching by Domain Walls in Ferri
W. Wiechec and C. M. Kelley (Stanf
Res. Inst.); *J. Appl. Phys.*, suppl. to vol.
pp. 131S–132S; May, 1960.

Experimental evidence indicates t
small grain size is associated with fa
domain wall switching in ferrite cores.
has been shown by H. Amar that small gr
size contributed an additional energy to
wall energy density σ_ω. Incorporation of
energy into the power equation $H\cdot(dM$
$=\lambda H_e^2$ reveals that the loss coefficient
creases more than σ_ω increases; theref
faster switching results. A qualitative
planation for faster switching by dom
walls in magnetic materials is given.
significant variables in the switching
efficient equation are "d", T_c, K, and α.
perimental data show that the switching
efficient is lowered by decreasing value
the first three variables. Considerably fa
switching is predicted when similar c
with grain sizes less than 1μ are used.

1025
Elastic Switching Properties of Some Squ
Loop Materials in Toroidal Structu
W. C. Seelbach and J. R. Kiseda (IBM R
Lab.); *J. Appl. Phys.*, suppl. to vol.
pp. 135S–136S; May, 1960.

Elastic switching properties of s
square loop materials are presented, and
concept of an elastic switching const
$S_{w(r)}$ is introduced. The plot of app
"turn over" field strength vs the inverse
the drive width indicates that the inela
switching constant for a given materia
four to five times greater than the ela
switching constant $S_{w(r)}$. The "turn ov
field strength is defined to be that valu
field strength at which inelastic switch
just starts and therefore is considered to
the upper limiting field strength for ela
switching. To a first-order approximati
the ratio of $S_{w(r)}$ to S_w is shown to be eq
to the percentage of the total flux capa
of the core that can be switched in an ela
mode of operation. $S_{w(r)}$ values for Mol
denum Permalloy ranged from 0.0
oersted μsec for $\frac{1}{8}$ mil tapes to 0.0913 oers
μsec for $\frac{1}{2}$-mil tape.

1026
Principles of Transfluxor and Core Circu
J. A. Rajchman (RCA); *Annals of the C*
putation Laboratory, Harvard Univer
Press, Cambridge, Mass., vol. 30, pp. 1
137; 1959.

The main principles underlying the o
ation of magnetic circuit elements, part
larly transfluxor and core circuits, are
scribed. Topics discussed include core m

es, shift registers, coders and decoders, rent steering in both cores and trans-xors, nondestructive transfluxor memories l multi-apertured transfluxors. Magnetic terial is shown to be eminently suitable storage and also convenient for switching en the number of elements or the number outputs is very large.

27
agnetic Analogs of Relay Contact Net-rks for Logic, D. B. Armstrong, T. H. owley, U. F. Gianola, and E. E. Newhall ell Telephone Labs., Inc.); IRE TRANS. ELECTRONIC COMPUTERS, vol. EC-9, pp. -35; March, 1960.

Two techniques for designing multi-erture magnetic structures capable of lizing any specific logic function are de-ibed. The structures are made from rec-ngular hysteresis loop material. The de-ns are derived from the corresponding re-contact network by replacing each cur-nt-carrying conductor in the relay circuit th its analog in the magnetic circuit, a x-carrying conductor; replacing the EMF th a pulsed mmf; and replacing each back ntact with a saturable portion of the mag-tic circuit in the topological equivalent of e contact network. A flux reversal through aturated portion may then be blocked by eans of an inhibiting current applied to a table winding, the current representing a ical input variable. Thus, flux may be eered" through the magnetic circuit in a nner analogous to the steering of current rough the contact network. For planar uctures, the first technique may be used obtain the analog of series-parallel and dge type circuits; the second technique is table only for the analogs of series-parallel cuits. It is pointed out that the analog of elay tree can be used as a standard struc-e suitable for realizing any Boolean func-n. Representative examples of both de-ns are shown, and experimental data are en.

28
w Multi-Aperture Magnetic Logic Ele-nt, D. R. Bennion (Stanford Res. Inst.); *Appl. Phys.*, suppl. to vol. 31, pp. 129S–0S; May, 1960.

A new magnetic multi-aperture device AD) having general logic capability is cribed. This device can be used for either ect or complementary transfer of binary rmation, depending only on a simple nge in wiring. AND and OR logic func-ns can be performed in the interconnect-circuitry, which consists only of con-ting wire. Significant operating toler-es have been exhibited by the new ele-nt, which is simpler in structure and ociated wiring than previous MAD's ving the same logic capability.

29
w Approach to High-Speed Storage— w Flux Density Materials, W. L. evel, Jr., and H. Chang (IBM Res. Lab.); *Appl. Phys.*, suppl. to vol. 31, pp. 125S–5S; May, 1960.)

A new approach toward overcoming the tors currently limiting the frequencies at ch storage devices may be switched from information state to another is presented. Ferrite elements for random-access storage which require a fraction of a microsecond for a cycle have been developed. Thus, the ferrite switching time establishes a maximum switching rate given by the inverse of the total switching time in a cycle. However, operation of elements such as these in a large capacity memory at rates limited only by switching times is usually prevented by: deterioration of magnetic properties due to heating effects, increase in selection line impedance, and long transmission delays. A series of ferrimagnetic oxides with properties such that the limits on minimum cycle time are appreciably extended have been developed. The most important of these properties is the saturation flux density. Over a range of composition, flux densities which extend from 100 500 gauss have been obtained. The lower flux density results in an appreciably lower energy dissipation in the magnetic structure and consequently in higher switching rates for a given temperature rise within the magnetic material. In addition, temperature dependence of those magnetic properties which determine storage applicability is more favorable than with the better known ferrites. Toroids which are suitable for random-access memories have been fabricated with these materials. These elements have been operated successfully in free air at repetition frequencies in excess of 2 Mc. The improvements in array characteristics that result are discussed in terms of impedances and transmission delays.

1030
Development of High-Speed Coincident Current Memory Cores, B. R. Eichbaum (Ford Motor Co.); *J. Appl. Phys.*, suppl. to vol. 31, pp. 117S–118S; May, 1960.

In present-day large computers the memory cycle is on the order of 8μsec, requiring memory cores to switch in 1.5 μsec with a full select drive of approximately 0.7 ampere. Memory cores suitable for use in such a computer can be fabricated from a $MgO \cdot MnO \cdot Fe_2O_3$ ferrite material. Using the same ferrite material, memory cores which have a switching speed of 0.4 μsec with a full select drive of approximately 1.0 ampere have been developed. The procedure used to fabricate these high-speed coincident current memory elements is described. The drive current is reduced to approximately 0.7 ampere when partial substitutions of CaO and Cr_2O_3 are made for MgO and Fe_2O_3, respectively, in the $MgO \cdot MnO \cdot Fe_2O_3$ core composition.

1031
Deposited Magnetic Films as Logic Elements, A. Franck, G. F. Marette, and B. I. Parsegyan (Remington Rand Univac); *Proc. EJCC*, pp. 28–37; December 1–3, 1959.

The logical properties of thin magnetic films are described and the use of functional-array logic in the scale factoring of a data word is explained in detail. The use of functional-array logic permits a great reduction in the time necessary to carry out operations which are sequential in nature.

1032
Chemically Deposited NiCo Layers as High Speed Storage Elements, R. J. Heritage and M. T. Walker (Royal Radar Establishment); *J. Electronics and Control*, vol. 7, pp. 542–552; December, 1959.

The preparation of layers of NiCo by chemical reduction is reported and their possible application for high-speed memory elements is discussed. Switching constants of 0.15 μsec oersted have been achieved on layers with domain wall coercivities of about 2 oersteds, and the process appears to give reproducible results. The method is simple and inexpensive and should be adaptable to the production of storage elements in large numbers.

1033
Operation of Magnetic Film Parametrons in 100- to 500-Mc Regions, A. V. Pohm, A. A. Read, R. M. Stewart, Jr., and R. F. Schauer (Iowa State University of Science and Technology); *J. Appl. Phys.*, supp. to vol. 31, pp. 119S–120S; May, 1960.

The behavior of thin magnetic films of Permalloy when used as time variable inductors is analyzed in terms of a modified Landau-Lifshitz equation. These results show that parametrons using time variable magnetic film inductors can be made to operate at reasonable power levels with large gains per cycle at oscillating frequencies in the 100- to 500-Mc region. The fabrication of magnetic film parametrons with strip line techniques is described. Calculations indicate that units with dissipations in the 10-mw range are feasible with existing techniques for operation in the 100- to 500-Mc region. Methods for advantageously using capacitive coupling between parametron units are discussed. These methods utilize the two new subharmonic states of a magnetic film parametron created by a bias reversal.

1034
Electrodeposited Memory Elements for a Nondestructive Memory, T. R. Long (Bell Telephone Labs., Inc.,); *J. Appl. Phys.*, suppl. to vol. 31, pp. 123S–124S; May, 1960.

Memory elements for a fast, nondestructive memory which consist of nickel-iron films electrodeposited onto a wire substrate are described. By plating in the presence of a directed magnetic field, an anisotropy favoring circumferential orientation is established. Axial interrogation fields cause reversible rotations of less than 90° and produce output signals across the ends of the wire. The apparatus and techniques used to make this wire are discussed together with the rationale of the design. The choice of alloy composition and the plating conditions strongly affect the results. The amount of stress in the deposit, the residual stress in the substrate, the control of precleaning of the substrate, the use of a suitable wetting agent, and the degree of stirring in the electrolyte appear as the vital factors in obtaining consistent results. Moderate fields ($\sim$30 oersteds) applied during plating produce a preferred circumferential orientation with high anisotropy ($H_K/H_0 = 3.0$). Squareness ratio in the easy direction is 0.99. Output signals appear during the rise time of the interrogation pulse with an amplitude inversely related to the rise time and directly proportional to the length interrogated. Very fast switching with unusually high output signals per unit length are possible.

Selective write-in is possible with current margins of 3:1. Preliminary investigations indicate that it would be feasible to make plated wire on a production basis with properties suitable for memory applications.

1035
The Crossed-Film Cryotron and Its Application to Digital Computer Circuits, V. L. Newhouse, J. W. Bremer and H. H. Edwards (General Electric Co.); *Proc. EJCC*, pp. 255–260; December 1–3, 1959.

A crossed-film cryotron deposited on an insulated superconductor is described. This CFC has a time constant of less than 1 μsec and is approximately one hundred times faster than the original vacuum-deposited cryotron. The dc dissipation is less than 5 microwatts and the active area of each element is approximately 5×10^{-4} square centimeters. These cryotrons and all their interconnecting circuitry can be vacuum deposited at one and the same time in a few simple steps. The cryotrons can be applied to both switching and storage. Some experimental storage and shift-register circuits are described, which demonstrate a circuit property unique to superconductors. A shift-register circuit is shown which is deposited in an area corresponding to 20,000 active elements per square foot. Calculations are presented which show that with this component density, a computer or memory containing more than one million elements can be accommodated in a one-cubic-foot liquid helium container using presently available refrigeration methods.

1036
The "Persistor"—A Superconducting Memory Element, E. C. Crittenden, Jr., and J. N. Cooper (U. S. Naval Postgraduate School) and F. W. Schmidlin (Space Technology Labs.); PROC. IRE, vol. 48, pp. 1233–1246; July, 1960.

A new computer memory element called the Persistor is described. The basic components of a Persistor are a superconducting inductor in parallel with a switch element which is normally superconducting, but which becomes resistive when the current exceeds a critical value. When a suitable current pulse is applied to a Persistor memory element, a persistent circulating current is stored. A second pulse in the same direction as the first makes no change, but a pulse in the opposite direction reverses the circulating current and produces a voltage across the element. By mutual inductance coupling to two or more driving circuits, these memory elements can be made to operate in matrices similar to those employed with ferromagnetic cores. Persistor memory elements utilizing lead inductors and thin tin or indium films have performed typical memory unit functions for pulses of 15-μsec duration and a repetition rate of 15 Mc. Performance at higher speeds is possible. The limiting speed is determined by the thickness of the thin film switch element and can be made as fast as is useful for the other parts of the associated circuits. The elements are well suited to compact printed circuit production with densities of a million per cubic foot possible.

1037
Chemical Switches, B. K. Green, E. Berman, B. Katchen, L. Schleicher, and J. J. Stansbrey (Natl. Cash Register Co.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 316–235; 1959.

Switches employing photochromic compounds and permselective membranes as elements are described. Essentially, photochromic phenomena may be considered as representing reversible photographic systems. Permselective membranes permit the passage of anions or cations but not both. By controlling the light incident on photochromic compounds or the charge on permselective membranes, switching systems may be synthesized. Practical means of developing such systems are indicated.

1038
Correction for Potentiometer Loading in Analog Computer Coefficient Potentiometers, E. H. Jakubowski (Springfield Armory); *U. S. Govt. Res. Repts.*, vol. 33, pp. 535–536 (A), May 13, 1960; PB 144 941 (order from LC Mi$3.00, Ph$6.30).

A set of tables containing correction factors which must be added to a potentiometer to compensate for loading due to an input resistor of finite value is presented. The procedure is described, and calculations are given.

A-3: EQUIPMENT—SUBSYSTEMS

1039
A Combined Counter and Decoder Using Transistors and Magnetic Cores, W. A. E. Loughhead, A. Kaposi, G. A. Matthews, and J. A. Woodward (Ericsson Telephones); *Proc. IEE*, vol. 106, pt. B, suppl. no. 18, pp. 1244–1250; May, 1959.

The operation of a counter in the "m out of n" code using transistors and magnetic cores is described. Its basic units are discussed, and the control of the pulse length of the driving and biasing stages is described in detail. It is shown that the counter is independent of the spreads of the transistor characteristics and variations in the supply voltage.

1040
The Design and Performance of a Hall-Effect Multiplier, R. P. Chasmar, E. Cohen and D. P. Holmes (Metropolitan-Vickers Electrical Co.); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 702–705, 746–747; May, 1959.

The construction of a Hall-effect multiplier is described and such design features as linearity, frequency response, temperature stability and circuit considerations are discussed. Applications of the device, including its use in analog computers, are suggested.

1041
The Sources of Error in Hall-Effect Multipliers, A. R. Billings and D. J. Lloyd (University of Bristol); *Proc. IEE*, vol. 106, pt. B, suppl. no. 16, pp. 706–713, 746–747; May, 1959.

The errors produced in a Hall-effect multiplier are examined and are shown to belong to one of two categories; either they are due to coupling between input or output, or they are produced by nonlinear process within the device. An estimate of the ma nitude of the errors is given and interprete in terms of carrier leak, modulation leak, ar envelope distortion for the particular appl cation of a Hall-effect modulator. Plat constructed of indium antimonide and i dium arsenide are compared on the bases carrier suppression, temperature stabilit conversion efficiency, and distortion. Carri suppressions of up to 80 db can be obtaine for both materials.

1042
Physical versus Logical Coupling in Mem ory Systems, J. A. Swanson (IBM Corp. *IBM J. Res. & Dev.*, vol. 4, pp. 305–31 July, 1960.

A memory system consisting of bistab static dissipationless units such as ferrite ferroelectrics, or cryotrons is considered. F a given amount of physical material th memory capacity may be increased by usi smaller volumes of the bistable material f each bit. If made sufficiently small, howeve the individual bits will become unreliab because of the influence of thermal agitati and quantum-mechanical tunneling pro esses. Some unreliability can be tolerate since it can be compensated by redundanc The optimum size of the individual bit, f maximum information storage, is evaluate If thermal agitation is the prime source errors, then the optimum-sized bit involv typically less than 100 of the independe cooperating units (electron spins, dipol etc.) which cause the bistability. The ma mization process concerns itself only wi the preservation of information and not wi possible methods of access to the individu bit. In particular, the maximization proce neglects complications in the coding equi ment needed to read in and out of memor

1043
High Density Digital Magnetic Recordi Techniques, A. S. Hoagland and G. Bacon (IBM Corp.); IRE TRANS. ON ELE TRONIC COMPUTERS, vol. EC-9, pp. 2–1 March, 1960.

The use of readback waveform synthes through "single pulse" superposition is di cussed. A comprehensive, yet general, rea back simulation program is described whi will automatically, for any characteris pulse, simulate all possible readback sign patterns and test them for specified readi logic as a function of bit density. Amplitud phase, peak, etc., sensing are compared ar the influence of parameter variation on pe formance is indicated. Good correlation wi experiment has been realized and ben time has been greatly reduced. The si nificance of pulse waveform is clearly r vealed and this study has provided a gui to head design (ring and probe), permitti the optimization of a total recording syste for high-density storage.

1044
A High Speed, Small Size Magnetic Dru Memory Unit for Subminiature Digit Computers, M. May, G. P. Miller, R. Howard, and G. A. Shifrin (Thompso Ramo Wooldridge, Inc.); *Proc. EJCC*, p 190–199; December 1–3, 1959.

The electrical and mechanical design

mall magnetic drum memory suitable for e in aircraft and missiles is discussed. A ckel-cobalt magnetic coating by the enner electrolysis process is utilized, inly because of its hardness and resistance wear. The drum, which has a capacity of ,000 twenty-bit words, has over-all dimen-ns of 3.7×3.7×7.4 inches.

45
multaneous-Access Matrix Storage Sys-ms, R. C. Minnick (Harvard Univer-y); *Annals of the Computation Laboratory,* arvard University Press, Cambridge, ass., vol. 30, pp. 144–148; 1959.

Methods whereby several words in a agnetic core memory may be simultane-sly addressed are described. In the first ethod I words may be addressed by reading the cores with $1/2(I^2+3I+2)$ sets wires; horizontal and vertical wires are tivated, and redundant input wires ap-opriately threaded inhibit the unwanted res. The method may be modified to re-ıce the number of selection wires and to low only one set of selection circuitry to ındle multiplanar systems. A third method a radio-frequency nondestructive read-out ocess.

046
Method of Storing Binary Information in errite Memory Cores with Nondestructive ead-Out, J. K. A. Olsson (Telefonak-ebolaget L. M. Ericsson); *Solid-State hysics in Electronics and Telecommunica-ns;* Academic Press, New York, N. Y., ol. 3, pt. I, pp. 404–410; 1960.

The 0-flux nondestructive ferrite core ad-out method in which the binary digits " and "0" are represented by the demag-tized state and a remanent state, respec-vely, of the core is described. The tech-que is useful in matrix systems which ilize direct word selection. Methods for riting the two digits are discussed and some easurements made on two different cores e presented. The low pulse currents re-uired in the read-out permit the use of tran-stor drive circuits. A small memory built a programming unit is briefly described and is pointed out that the 0-flux method akes possible a trinary memory element if oth remanent states and the demagnetized ate are used.

047
Transistorized Magnetic-Core Store, . Bray and A. C. Conway (E.M.I. Elec-onics); *Proc. IEE,* vol. 106, pt. B, suppl. o. 16, pp. 644–648, 698–701; May, 1959.

A transistor-driven magnetic-core store aving a capacity of 4096 words, each of 37 ts, which was developed for a large transis-rized computing system is described. The ive currents are generated in a central enerator, and address selection is achieved transistor gating circuits. A typical store rcle-reading followed immediately by riting requires 12 μsec with random cess.

048
Miniature Memory Planes for Extreme En-ronmental Conditions, R. Straley, A. euer, B. Kane, and G. Tkach (Indiana General Corp.); *J. Appl. Phys.,* suppl. to vol. 31, pp. 126S–128S; May, 1960.

Ferrite memory planes which are highly compact and can operate over the temperature range −55°C to +125°C are described. Small size results from the use of a "continuous wire" method of inserting drive lines through memory planes and then folding the planes. This method eliminates the conventional frames and all solder connections between planes, increases reliability, and facilitates assembly of stacked memory planes. A typical folded stack of memory planes occupies as little as 2 per cent of the volume of its conventional counterpart. The new miniature memory stacks perform as well as conventional units. The development of ferrite memory cores operable at ambients as high as 85°C, 100°C, and 125°C (together with the greatly reduced volume of the memory stack) allows operation under extreme environmental conditions with a minimum of space and power requirements. The folded memory planes are packaged with a heating element and control circuit which maintain the temperature of the cores at the maximum ambient. A tested prototype of twelve 16×16 memory planes, along with the heating element and control circuit, measures 2 inches×2½ inches×2½ inches and has been successfully operated in the temperature range −55°C to +125°C. Ferrite cores of both the "fast" relatively high drive and relatively "slow" lower drive type have been perfected. They are Mg-Mn ferrites with possible minor additions of other bivalent oxides.

1049
A Fast Random-Access Diode-Capacitor Store Using Transistors, A. C. Conway (E.M.I. Electronics); *Proc. IEE,* vol. 106, pt. B, suppl. no. 16, pp. 657–662; May, 1959.

A fast random-access store using two semiconductor diodes and a capacitor to store each binary bit is described. At present, the store consists of 64 words of 38 parallel bits, with a random-access cycle time at any selected address of 4 μsec. The design of the selection circuits is described, including a reference to the use of transistors to produce voltage pulses of either polarity having well-defined amplitudes. Reference is made to the sensing and writing circuits, and also to the selection of diodes for use in the storage elements. In addition, information on reliability during operation is given.

1050
The Woven Cryotron Memory, A. E. Slade (Arthur D. Little, Inc.); *Annals of the Computation Laboratory,* Harvard University Press, Cambridge, Mass., vol. 30, pp. 326–333; 1959.

The basic principles of a cryogenic parallel access read-only woven memory are described. Each word is represented by a unique pattern of superconductive wire woven in the memory. Such a memory is essentially a giant comparator in which any random input may be compared with the entire storage simultaneously. The weaving technique for constructing such a memory is extremely simple. Obvious applications are the storage of large semipermanent random access catalogs and function tables.

1051
Magnetic Selectors, M. Karnaugh (Bell Telephone Labs.); *Annals of the Computation Laboratory,* Harvard University Press, Cambridge, Mass., vol. 30, pp. 186–191; 1959.

The main types of magnetic selectors and stepping switches for controlling access to core memory arrays are described. Use of coincident-voltage output networks makes it feasible to select one of up to 1000 outputs, and hence to give access to very large coincident current memory arrays.

1052
A Code Translator for Letter-Sorting Machines, J. D. Andrews (Post Office Engrg. Dept.); *Proc. IEE,* vol. 196, pt. B, suppl. no. 16, pp. 637–643; May, 1959.

A transistorized code translator aimed at reducing the memory required for manual or machine sorting of mail is described. The translator employs a matrix of 5×26 rectangular B/H loop cores to translate a five (or less) alphabet character code, derived from the address on the envelope, into one of 144 possible output signals. The maximum capacity of the present translator is about 4000 five-character codes.

1053
A Silicon Transistorized Scaling Stage, L. B. Gardner (Litton Industries); IRE Trans. on Instrumentation, vol. I–9, pp. 55–59; June, 1960.

The design, packaging, and evaluation of a scaling stage which utilizes silicon transistors, thereby achieving stable operation at temperatures in excess of 110°C, is presented. The relative advantages and disadvantages of operating the semiconductors in the saturated or nonsaturated region is discussed and several practical circuits of each type are given. From laboratory measurements it appears that for a nonsaturated fast flip-flop, the output transient response is independent of the input transient response. An hypothesis for explaining this phenomenon is given along with the description and conclusions of controlled experiments designed to test the hypothesis. In these experiments several circuits which differed only in the manner of preventing saturation were examined. In all of the devices, only readily available production components were employed. The finally evolved unit is characterized by output rise and fall times of 15 millimicroseconds or less, a delay time of less than 20 millimicroseconds, and a resolution time of less than 50 millimicroseconds for pulse triples. Photographs, circuit diagrams, and typical waveforms of this unit are presented, along with applications of the device to nuclear instrumentation and computer logic.

1054
The Use of Transistors in a Digital Correlator for Processing Radar Information, A. L. Cain, P. Swift, and A. T. Watts (Mullard Res. Labs.); *Proc. IEE,* vol. 106, pt. B, suppl. no. 16, pp. 649–656; May, 1959.

A transistorized digital system for improving the signal/noise ratio of a search radar by correlating the responses from several successive transmitted radar pulses

is described. The main emphasis is on the circuit techniques employed. The radar information is first quantized into 2 levels of amplitude ("0" and "1") and then into 1024 range elements of $\frac{1}{4}$ nautical mile each, *i.e.* 3.09 μsec. The correlation is achieved by counting the "1's" stored at each range for a number of consecutive radar PRF periods and deciding whether or not the results are significant. The criteria chosen for this should enable the system to have an over-all bearing accuracy somewhat better than the antenna beamwidth. Four separate correlation circuits are used, each handling every 4th range quantum. Thus the clock period is 12.4 μsec, which allows the use of standard magnetic-core-storage techniques. The machine is entirely transistorized. The circuits described include 1) a precision 323-kc triggered LC oscillator, 2) high-speed logical circuits using transistors and diodes, 3) a high-speed reversible counter and 4) parts of the storage system.

1055

Feasibility Study for a Keyboard Type Selector Plugboard and Plugboard Checker, R. E. Michaud (Computer Control Co., Inc.); *U. S. Govt. Res. Repts.*, vol. 33, p. 535 (A), May 13, 1960; PB 137 513 (order from LC Mi$4.50, Ph$12.30).

The feasibility of replacing a plugboard method of connecting logical elements by an automatic method using a paper tape or a keyboard is discussed. Two possible means of implementation are considered: the telephone crossbar and the magnetic transfluxor with associated electronic circuits. The transfluxor is adjudged to be superior, and a demonstration unit constructed to illustrate the logical design and circuit techniques involved is described.

A-5: EQUIPMENT—ANALOG COMPUTERS

1056

Frequency-to-Period-to-Analog Computer for Flowrate Measurement, T. W. Berwin (University of California); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-9, pp. 62–71; March, 1960.

The Frequency - to - Period - to - Analog Computer, a special-purpose nonlinear analog computer which accepts an ac voltage of varying frequency, acts upon the period of each cycle, computes the inverse of the time period, $e=1/T$, and holds the information for the period of the next cycle, is described. The output voltage is a level which is proportional to the input frequency $f=1/T$ computed once for every cycle. The system is accurate to better than ± 0.5 per cent of $\frac{2}{3}$ full scale. Application of the computer is discussed and results for fast readout and recording of gas and liquid turbine type flowmeters are presented. Extensions of the circuits used can produce voltages proportional to $\ln t$ or $1/t^2$, for time t greater than a small positive number.

A-6: EQUIPMENT—ANALOG-DIGITAL COMPUTERS

1057

A Combined Analog-Digital Differential Analyzer, H. K. Skramstad (Natl. Bur. Standards); *Proc. EJCC*, pp. 94–100; December 1–3, 1959.

An analog-digital differential analyzer which combines the analog advantages of high speed and continuous representation of variables with the digital capability of high precision and dynamic range is described. It is based on representing dependent variables by two quantities, a digital number representing the more significant part and an electrical voltage representing the less significant part. As in the electronic analog computer, time is the independent variable. The design of components such as integrators and multipliers required to build a computer of this combined type is given and examples of the solution of a few elementary differential equations are presented.

1058

A 2-Channel Data Link for Combined Analog-Digital Simulation, J. Greenstein (Convair); *Commun. and Electronics, (Trans. AIEE*, vol. 79, pt. I), no. 47, pp. 40–44; March, 1960.

Following a discussion of the characteristics of digital and analog computers, a two-channel data link for connecting a digital computer (the Sperry Rand ERA 1103) and an analog computer (550 operational amplifier analog computer) is described. The application of the data link is illustrated in the real-time simulation of a guided missile system. The link permits a more realistic simulation than is otherwise possible. Several other advantages of the arrangement are also pointed out.

1059

Conversion Between Analogue and Digital Measures, R. H. Tizard (Associated Electric Industries Ltd.); *Computer J.*, vol. 3, pp. 51–59; April, 1960.

The text of an introductory lecture which enumerated the principles and standard techniques of analog-digital conversion is presented. Many of the more common mechanical and electrical methods are described. Among the topics considered are sampling, filtering, and coding.

B-1: SYSTEMS—THEORETICAL DESIGN

1060

Optical Data Processing and Filtering Systems, L. J. Cutrona, E. N. Leith, C. J. Palermo, and L. J. Porcello (University of Michigan); IRE TRANS. ON INFORMATION THEORY, vol. IT-6, pp. 386–400; June, 1960.

Optical systems, which inherently possess two degrees of freedom rather than the single degree of freedom available in a single electronic channel, appear to offer some advantages over their electronic counterparts for certain applications. Coherent optical systems have the added property that one may easily obtain many successive two-dimensional Fourier transforms of any given light amplitude distribution; or, by use of astigmatic optics, one-dimensional transforms can be obtained. Therefore, most linear operations of an integral transform nature are easily implemented. The optical implementation of integral transforms which are of importance to communication theory is discussed; the general problems of optical filter synthesis and multi-channel computation and data processing are introduced, followed by a discussion of potential applications. Astigmatic systems, which perm multi-channel operations in lieu of tw dimensional processing are treated as special case of general two-dimensio processors. Complex input functions are d cussed with relation to their role in cohere optical systems. [See also IRE TRANS. AUTOMATIC CONTROL, vol. AC-4, pp. 13 149; November, 1959.]

B-2: SYSTEMS—DESCRIPTIONS

1061

The System Organization of Mobidic S. K. Chao (Sylvania Electric Product *Proc. EJCC*, pp. 101–107; December 1- 1959.

MOBIDIC B, an all-transistorized mi tarized computer mounted in a standa army trailer, is described. It is a general-pi pose, parallel, binary synchronous, fix point, and duplexed data processing syste containing two basic processors identical characteristics internally tied together to t same system transfer bus. Both process share a common set of input-output devi and each is capable of operating an ind pendent program without interference. Th are also capable of duplexed operation, lowing either processor to monitor and ex control over the other. In addition to t 8192-word high-speed core memory in ea processor, there exists a 50 million-bit m memory. This memory is treated as an inpu output device, addressable by in-out instru tions. A data retrieval unit is incorporated facilitate data searching from the magne tape and mass memory.

1062

A Mobile General-Purpose Data-Processi System, C. Pilnick (Consolidated A onics); IRE TRANS. ON INSTRUMENTATIO vol. I–9, pp. 35–39; June, 1960.

A mobile data-processing system suital either for expansion of existing telemet data reduction facilities or as an independe data processor at remote test areas is d scribed. The equipment is mounted in forty-foot, air-conditioned van, and includ facilities for acquiring data from a wi variety of transducers, conditioning a normalizing signals, recording in both anal and digital form, processing selected cha nels for entry into an IBM 704 comput data editing and tabular printout. The sy tem will accept inputs as low as one milliv full-scale, and is designed for use with maximum of 216 input data channels rep senting signals from variable reluctan strain gauge bridge, thermocouple, poten ometer, flow rate, acoustic and accelerome transducers. Recording instrumentation m dia include digital and analog magnetic ta punched paper tape, electric typewrit direct-writing oscillographic recorders, str chart recorders, and visual presentati from both digital and analog voltmete Special design and construction techniqu necessary for reliable operation under mob conditions are described.

1063

Bendix G-20 System; *Commun. Assoc. Comp. Mach.*, vol. 3, pp. 325–328; May, 19

The main specifications, order structu and operating characteristics of the Ben

) general purpose, automatic data proc-
ng system are presented. A standard
ine called Monitor controls input-output
rations, permits the concurrent operation
wo or more programs, and automatically
dules the use of peripheral equipment on
basis of a priority program selected by
user.

4
s—A New Concept in Large Computer
ign; *Commun. Assoc. for Comp. Mach.*,
3, pp. 367–368; June, 1969.
The main features of ATLAS, a new large-
e computer developed jointly by the
versity of Manchester and Ferranti,
., are described. Newly developed adding
uits reduce the average time for a 48-bit
ting point addition to 1.1 per second.
h section of 4096 word core memory
rates independently with a cycle time of
ec. Rapid fixed storage is provided by a
en wire mesh with ferrite slugs at inter-
ions, and the back-up storage is mag-
c drums and tape. Sophisticated multi-
gramming facilities are provided.

5
ce Data Processing System, L. P.
pene, Jr. (Melpar, Inc.); *U. S. Govt. Res.*
ts, vol. 33, p. 535 (A), May 13, 1960;
144 797 (order from LC Mi$6.30,
19.80).
The system programming, the results of
asibility study, and the design and de-
pment of transistorized plug-in modules
a digital voice data processing system
presented. This system, being fabricated
upport the development of a speech band
th compression technique, is a special
pose computer operating from a 400-kc
k. Several operational modes are pro-
ed to enable use of the voice data process-
system as a data accumulating and
ing device and then as a complete com-
nication system simulator. A mathe-
ical design analysis and a description of
rational evaluation tests for one of the
uit modules are included as appendices.

B-3: SYSTEMS—APPLICATIONS

5
**Multi-Sequence Computer as a Com-
nications Tool,** J. N. Ackley (Internatl.
ctric Corp.); *Proc. EJCC*, pp. 114–119;
ember 1–3, 1959.
Possible applications as a communica-
s tool of a multisequence computer in
ch more than one sequence or program
rates independently, time-sharing the
ral processing unit, are discussed. The
puter is made to time-share on an on-
and basis between all of the input and
put devices. The control sequences and
buffering can be provided by the central
cessing unit. A multi-sequence computer,
ch permits economical integration of a
tiplicity of input and output devices,
omes a very rapid and economical mes-
e switching center by connecting the
munications lines as the input and out-
devices. This configuration can also be
loited as a real time data processing sys-
or a real time control system.

C-2: AUTOMATA—ARTIFICIAL

1067
The Logic of Fixed and Growing Automata, A. W. Burks (University of Michigan); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 147–188; 1959.

Discrete, synchronous, deterministic computers are referred to as automata. Several languages for describing automata and methods for transforming expressions from one language to another are presented and some general theorems concerning automata are proved. Precise definitions for fixed and growing automata are offered and a distinction is made between bounded growing automata such as the human brain, the thresholds of whose neurons change with time, and unbounded automata, such as Turing machines. A computer with indefinitely extensible tapes is an example of a growing automaton. [See also U. S. Govt. Res. Repts., vol. 33, p. 535 (A), May 13, 1960; PB 144 660 (order from LC Mi$3.00, Ph$6.30).]

1068
Regular Expressions and State Graphs for Automata, R. McNaughton and H. Yamada (University of Pennsylvania); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-9, pp. 39–47; March, 1960.

Algorithms for 1) converting a state graph describing the behavior of an automaton to a regular expression describing the behavior of the same automaton and 2) for converting a regular expression into a state graph are presented. These algorithms are justified by theorems, and examples are given. A brief introduction to state graphs and the regular-expression language is also given.

D-1: PROGRAMS—AUTOMATIC PROGRAMMING, DIGITAL COMPUTERS

1069
Some Remarks on the Game "Dama" Which Can Be Played on a Digital Computer, N. V. Findler (Colonial Sugar Refining Co. Ltd.); *Computer J.*, vol. 3, pp. 40–44; April, 1960.

The strategies employed in programming the computer SILLIAC to play the Middle-European game Dama, akin to checkers, are described. A learning process whereby an optimal grand strategy can be achieved is suggested. The techniques employed have application in the general field of intelligence simulation.

1070
A Start at Automatic Storage Assignment, R. L. Patrick; *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 321–322; May, 1960.

A technique whereby sets of equations can be arranged in computational order and checked for computability is described. The technique indicates what equations can be handled in parallel (assuming one has parallel arithmetic facilities) or can be considered a logical entity. An efficient allocation of high-speed memory is also determined, so that memory is reassigned as soon as its immediate duties are fulfilled.

1071
Multiprogram Scheduling. Parts 1 and 2. Introduction and Theory, E. F. Codd (IBM Corp.): *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 347–350; June, 1960.

In order to exploit fully a fast computer which possesses simultaneous processing abilities, the computer should to a large extent schedule its own workload. The scheduling routine must be capable of extremely rapid execution if it is not to prove self-defeating. The construction of a schedule entails determining which programs are to be run concurrently and which sequentially with respect to each other. A concise scheduling algorithm which tends to minimize the time for executing the entire pending workload (or any subset of it), subject to external constraints such as precedence, urgency, etc., is described. The algorithm is applicable to a wide class of machines.

1072
Report on the Algorithmic Language Algol 60, P. Naur, *et al.; Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 299–314; May, 1960.

A complete description of Algol 60, the latest version of the algorithmic language Algol, is presented. Three different levels of language are recognized, namely, a reference language, a publication language, and several hardware representations. A catalog of the symbols of the reference language is provided.

1073
The Optimal Organization of Serial Memory Transfers, A. Gill (University of California); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-9, pp. 12–15; March, 1960.

The optimal compilation of programs whose function is to transfer words of information from one location in a serial memory to another is considered. The most important optimization tool is the "timing schedule," which facilitates the analysis of various transfer schemes and the determination of the fastest one. The procedure described for optimizing serial transfers is readily programmable for computer execution and is directly applicable to a general class of transportation problems.

1074
Compiling Connectives, C. J. Swift (Computer Sciences Corp.); *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 345–346; June, 1960.)

The operation of the Honeywell 800 compiler in translating connectives from a FACT language to machine language is described. The FACT language is adapted to accept as many uses of connectives in everyday English as possible. The compiler operates on connectives by expanding the original source statements to generate an equivalent statement in which connectives connect only complete conditional or imperative clauses.

1075
Simcom—The Simulator Compiler, T. G. Sanborn (Space Technology Labs., Inc.); *Proc. EJCC*, pp. 139–142; December 1–3, 1959.

SIMCOM, a program for generating computer simulation programs to be run on an IBM 709 computer, is discussed. SIMCOM accepts statements written in a specialized simulation-oriented language and generates, in SCAT language, instructions similar to those prepared by a human programmer during the preparation of a simulation program. SCAT instructions are generated from SIMCOM statements with a single pass through the source program.

D-2: PROGRAMS—APPLICATIONS, DIGITAL COMPUTERS

1076

The First Year's Experience With a Large Computer in a Life Assurance Office, R. L. Sutton (Confederation Life Assoc., London); *Computer J.*, vol. 3, pp. 2–9; April, 1960.

The simultaneous conversion of all ordinary policy operations from manual handlings to an electronic data processing system for a large life assurance office is described. The first year's experience of the system, including the problem of transatlantic transportation of input data and results, is commented on. The disadvantages encountered are considered to be of a superficial nature and easily rectifiable.

1077

Problems of Auditing Computing Data: Internal Audit Practice and External Audit Theory, T. R. Thompson (LEO Computers Ltd.) and F. C. de Paula (Robson Morrow and Co.); *Computer J.*, vol. 3, pp. 10–14; April, 1960.

The auditing problems associated with the widespread commercial use of electronic data-processing systems are discussed. New methods of both internal and external audit to replace manual checks against error and fraud are described. Careful authorization of alterations to programs, special spot-checking programs, a security copy of all print-outs, and more frequent attendance of auditors are among the means advocated.

1078

Data Processing in University Administration, P. F. Windley, L. R. Kay, and A. Rowland-Jones (University of Leeds); *Computer J.*, vol. 3, pp. 15–20; April, 1960.

The initial stages of handling student records on an electronic data processing system are described. Extremely rapid preparation and processing of the relevant data on each student are necessary to ensure that the resulting output is of maximum utility to both faculty and administration staff. Among the benefits realized are the earlier distribution of lists and statistics and the reduction of clerical labor and of routine work falling on faculty members.

1079

Computers in Medical Data Processing, R. S. Ledley (George Washington University) and L. B. Lusted (University of Rochester); *Operations Res.*, vol. 8, pp. 299–310; May-June, 1960.

The ideas inherent in the utilization of digital electronic computers in medical data processing are briefly summarized. Concepts associated with the application of a sequential decision theory to the analysis of medical diagnosis and with the accumulation and recall of individual medical records are discussed. It is concluded that the importance of a national health computer network cannot be overestimated, both as an aid to increasing individual good health and longevity and as a vast new source of medical information concerning mankind. Present-day computer technology indicates that such a health computer network is entirely feasible.

1080

The Automatic Digital Computer as an Aid in Medical Diagnosis, C. B. Crumb, Jr. (Bendix Aviation Corp.) and C. E. Rupe (Henry Ford Hospital, Detroit); *Proc. EJCC*, pp. 174–180; December 1–3, 1959.

It is suggested that by means of a statistical correlation technique digital computers can greatly improve medical diagnostic procedures. Correlation constants which express the probability of the association of each symptom with each disorder would be stored in the bulk storage of the computer. Suspected disorders and observed or reported symptoms would be placed in the computer working storage. For each disorder the appropriate table of correlation constants would be extracted from the bulk storage and transferred to the working storage. The constants would then be modified if necessary and the appropriate ones summed up to give the relative probability index numbers. The disorder with the largest index number should be the correct diagnosis or the one with the highest correctness probability. The computer requirements are discussed and it is pointed out that the storage of data in the computer memory will result in more reliable correlation constants than are now available.

1081

Train Performance Calculated by Digital Computer—Supplemental Programs, J. E. Hogan (Pennsylvania Railroad Co.); *Applications and Industry*, (*Trans. AIEE*, vol. 79, pt. II), no. 48, pp. 114–118; May, 1960.

Two programs for the preparation of data required in an IBM-650 program for calculating train performance are described. The MALT (maximum acceleration on level, tangent track) calculating program and the track data finalizing program greatly reduce the time required to prepare the preliminary data.

1082

Industrial Computers for Tank Farm Inventory Control and Data Handling, E. B. Turner and R. J. Noorda (General Electric Co.); *Elec. Engrg.*, vol. 79, pp. 390–393; May, 1960.

The use of a general-purpose, digital, stored-program computer for the collection and processing of data from the storage facilities of a large tank farm is discussed. The major functions which the computer must perform are listed and the equipment necessary to perform these functions is described.

1083

The Solution of Simultaneous Ordinary Differential Equations Using a General Purpo Digital Computer, W. H. Anders (Bendix Aviation Corp.); *Commun. Ass for Comp. Mach.*, vol. 3, pp. 355–360; Jur 1960.

The program for solving a set of simu taneous ordinary differential equations divided into two sections, namely integr tion and function evaluation. Means for t effective use of machine storage are d scribed, and an analysis of the truncati error for a Runge-Kutta type procedure provided.

1084

Transferability of Urey-Bradley Force Co stants I. Calculation of Force Constants or Digital Computer, J. Overend and J. Scherer (Dow Chemical Co.); *J. Chem. Phy* vol. 32, pp. 1299–1295; May, 1960.

A program for the calculation of Ure Bradley force constants on the Datatron 2 digital computer is described. The secu equation is set up and solved in internal ordinates, the potential energy being tra formed from Urey-Bradley space to intern coordinate space by a matrix Z. This sa matrix is also used to transform the Jacobi of λ with respect to the force constants fr internal-coordinate to Urey-Bradley spa thereby allowing the direct determination Urey-Bradley force constants. A meth whereby the Z matrix and Wilson's G mat may be set up by the computer from the g metrical parameters of the molecule described.

1085

New Ray Tracing Scheme, P. W. Fo (University of Tasmania); *J. Opt. Soc. A* vol. 50, pp. 528–533; June, 1960.

A detailed theoretical treatment of a n algebraic ray-tracing scheme for tracing ra from an object point through any axia symmetrical optical system, including ca dioptric systems which contain spheri surfaces only, is given. The coordinate s tems utilized are explained and an exam of a skew ray trace through a wide an system is presented. A Deuce computer h been programmed for this ray trace, a details of this program are given. A p determined scan interval is given to t machine which then proceeds automatica to trace from an object point rays spaced this interval over the first polar tange plane. For pencils of all obliquities, vign ting is carried out by the machine, wh produces as one of the results the appare shape of the entrance pupil.

1086

Unusual Techniques Employed in He Transfer Programs, D. J. Campbell a D. Vollenweider (General Electric Co *Proc. EJCC*, pp. 143–147; December 1- 1959.

An IBM 704 program for solving tran ent and steady state heat transfer proble is described. The program permits t analysis of three-dimensional problems w arbitrary geometry and several combin modes of heat transfer. An unusual meth of describing geometry and of presenting put data in symbolic form is discussed.

ts of input processing, testing, and anization are described. Further extens of these methods and computational niques are proposed.

7

utions of the Shortest-Route Problem—Review, M. Pollack and W. Wiebenson anford Res. Inst.); *Operations Res.*, vol. 8, 224–230; March-April, 1960.

Several methods for determining the rtest route through a network are debed and their relative merits are dised. Most of the methods are intended for nual and digital computation; however, analog methods are included. The dual between the shortest-route problem and network capacity problem is briefly ntioned.

8

Evaluation of AM Data System Pernance by Computer Simulation, R. A. by (Bell Telephone Labs., Inc.); *Bell . Tech. J.*, vol. 39, pp. 675–704; May, 0.

The mathematical relationships that debe an amplitude-modulated data system developed in a form suitable for prommming on a high-speed digital computer. ese equations contain expressions that cify in general terms the transmissionquency characteristics of a transmission dium. A data signal composed of a train aised-cosine shaped pulses is generated in erated in the simulating process. The ulation provides a means for computing resulting response of systems to pulse ns. The performance of a double-sided AM data system is evaluated from asurements of the maximum vertical ning, or aperture, of the eye pattern med by the received signal. This aperture related to the system performance in ns of signal-to-noise ratio and error rate he system. A verification of this techue is made by simulating the conditions n experimental laboratory data system the computer and comparing computed measured performance.

9

nputation of the Equilibrium Composi- of Burnt Gases, R. L. Potter and Vanderkulk (Bell Aircraft Corp.); *J. m. Phys.*, vol. 32, pp. 1304–1307; May, 0.

The multicomponent chemical equilibn composition problem is discussed genlly and is formulated suitably for digital puter calculations. A geometric interpreon of the equations used to specify the mical system is also given.

0

nbined Analog-Digital Simulation of Enering Problems, F. W. Pruden tl. Res. Labs., Ottawa); *U. S. Govt. Res. its.* vol. 33, p. 535 (A), May 13, 1960; 144 887 (order from LC Mi$2.40, 3.30).

A simple but realistic dynamic system is sidered, and the relative advantages of og and digital methods of solution are stigated. For solution accuracy limited to 4 decimal digits, the analog method heaper. However, for certain mathematical operations such as long-term integration and generation of complicated functions, digital computer accuracy may be necessary. The coupling of analog and digital machines is discussed, and the relevant sampled-data theory is introduced. The stability of such combined systems in calculations is considered. Finally some examples of combined calculations are given.

1091

The Analysis of Large Structural Systems, R. K. Livesley (University of Cambridge); *Computer J.*, vol. 3, pp. 34–39; April, 1960.

A technique for analyzing large structural frames on an electronic computer is described. The technique is of more general application and is suitable for electrical network analysis. Since the matrices involved in the calculations are sparse, the solution is speeded up by solving a number of subsystems and matching these solutions together. A principal feature of the technique is a packing system for the efficient storage of large submatrices.

1092

Digital Simulation of a Massed-Bomber, Manned-Interceptor Encounter, L. Brotman and B. Seid (Hughes Aircraft Co.); *Operations Res.*, vol. 8, pp. 421–423(L); May-June, 1960.

A program for simulating on the IBM 704 digital computer the performance of an advanced-type manned-interceptor weapon system against a massed raid of enemy bombers is reported. The program can accommodate a maximum of 250 interceptors and 500 bombers. Particular emphasis in simulating this problem was placed on close conformity to reality and sufficient flexibility for the handling of many different situations

1093

Computers and Change-Ringing, D. G. Papworth (University of Durham); *Computer J.*, vol. 3, pp. 47–50; April, 1960.

The rules of allowable permutations that define the sequences of bells to be rung in change-ringing on church bells are described. A program for the generation of new sequences on a Ferranti Pegasus computer is outlined and its results are appraised.

1094

The Mathematical Model Approach to Computer Control, D. B. Brandon (Thompson-Ramo-Wooldridge Products Co.); IRE Trans. on Industrial Electronics, vol. IE-7, pp. 15–20; March, 1960.

Two quite different bases for establishing an on-line computer control system for a manufacturing process have been described in the literature. These are the "exploratory" or "teleological" approach employing a mathematical model of the process. Both methods, when applicable to a particular plant installation, lead to considerably improved process control. In an effort to clarify the kind of situation in which predictive control is to be preferred, the major criteria are presented and described in general terms. Emphasis is placed on the requirements of plants in the chemical, petrochemical, petroleum, and similar industries. The elements of a predictive control system for a chemical-type plant are outlined.

1095

Prime Number Coding for Information Retrieval, A. H. Cockayne and E. Hyde (Imperial Chemical Industries, Ltd.); *Computer J.*, vol. 3, pp. 21–22; April, 1960.

A technique of coding file items by assigning a prime number to each property that can be possessed by an item is described. The number coding an item is the product of the primes coding the properties that the item possesses. When any particular item possesses a small proportion of the total allowable number of properties, the system is more economical in storage space and in search time than a system in which one bit is assigned to each property. To determine whether an item possesses a certain property its code number is divided by the corresponding prime and the remainder is tested for equality with zero. The system is applied to a file of organic chemical compounds.

1096

A Character-Recognition Study, W. E. Dickinson (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 335–348; July, 1960.

A study of the single-gap-scan approach to character recognition, using an IBM 650 for simulation, is reported. Ten specially designed digits were used in this study. Character recognition is discussed in terms of some simple concepts from n-dimensional geometry. The main contribution is an effective method for using a computer to aid in the design of the type font. This procedure is a natural development of the vector approach. Experimental results show the sensitivity of the system to phasing. An expression for a "quality factor" is given and the relationship of this factor to errors and to ink density is illustrated.

1097

Optimization of Reference Signals for Character Recognition Systems, I. Flores (Dunlap and Associates, Inc.) and L. Grey (Teleregister Corp.); IRE Trans. on Electronic Computers, vol. EC-9, pp. 54–61; March, 1960.

The role of signal structure in a signal discrimination system is discussed. The optimality criterion for reference signals for detection in the case of white Gaussian independent noise is defined. The need for normalization of the reference signals is demonstrated and a geometric interpretation is presented. Optimum classes are obtained and several examples are cited. A theoretical optimum class of signals is derived against which any set of signals developed within given constraints may be rated.

1098

A Method for the Design of Pattern Recognition Logic, S. D. Stearns (Sandia Corp.); IRE Trans. on Electronic Computers, vol. EC-9, pp. 48–53; March, 1960.)

The general problem of pattern recognition is regarded as a problem wherein the recognition device is presented with a plane array of black-or-white elements and must decide to which general class (pattern) this array belongs. A method for reducing the necessary amount of logic, which is basically a method for reducing Boolean equations in many variables which contain large numbers of redundant or "don't care" terms, is pre-

sented. The reduced logic is in the form of Boolean functions of the black-or-white elements. Some experimental results, in which this logic has been mechanized with diodes are discussed.

1099
The Automatic Transcription of Machine Shorthand, G. Salton (Harvard University); *Proc. EJCC*, pp. 148–159; December 1–3, 1959.

It is suggested that speech can be provided as machine input by utilizing a stenographic transcript. A brief description of the stenotype machine is given. The basic rules of stenotype and problems of stenotype translation are considered, and programs for the production of pseudo-English on the UNIVAC I computer are described. Many programs originally written for automatic Russian to English translation were found useful. In some cases, however, small alterations to the original programs were necessary.

D-3: PROGRAMS—TECHNIQUES, DIGITAL COMPUTERS

1100
Solving Noise Problems in Digital Computer Memories, A. H. Ashley and E. U. Cohler (Sylvania Electric Products, Inc.); *Electronics*, vol. 33, pp. 72–74; March 25, 1960.

The use of a drive-sampling core in the transistorized memory of MOBIDIC computer to generate strobe pulses more precisely defined than those generated by fixed strobe pulses is discussed. This new technique produces optimum strobe time in spite of variations in temperature, circuit delay, and drive current waveform. Strobe pulse, which is sensitive not only to the time at which current starts, but also to the waveform of the current, is produced by the ONE output of a memory core which has the same drive as the selected memory word.

1101
Abbreviating Words Systematically, J. A. Barrett and M. Grems (IBM Corp.); *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 323–324; May, 1960.

A systematic method of abbreviating words or phrases to specified computer word size is described. Detailed rules for the order in which the letters in a word should be removed are provided. The most important are that the first letter of a word is always to be retained, and the remaining letters are removed according to a frequency scale, starting from the right-hand end of the word.

1102
Automation of Computer Panel Wiring, G. W. Altman, L. A. de Campo, and C. R. Warburton (IBM Corp.); *Commun. and Electronics* (*Trans. AIEE*, vol. 79, pt. I), no. 48, pp. 118–125; May, 1960.

A "design mechanization" program written for the IBM 704 and 705 computers which prepares back-panel wiring lists for developmental data processing machines is described. The back-panel wiring lists describe how the circuit components are connected to perform logic and provide bills of material and other production control information. The program reduces the two engineering man-weeks previously required to produce a wiring list for a panel to 30 minutes of computer time and 6 hours of key punching and verification.

1103
Solution of Simultaneous Linear Equations Using a Magnetic Tape Store, D. W. Barron and H. P. F. Swinnerton-Dyer (Cambridge University); *Computer J.*, vol. 3, pp. 28–33; April, 1960.

The problems involved in solving a set of simultaneous linear equations when magnetic tape is used for auxiliary storage is described. A technique based on Gaussian elimination that uses row storage is presented. Means of checking intermediate results and of minimizing the number of word transfers are discussed.

D-4: PROGRAMS—TESTING, DIGITAL COMPUTERS

1104
Interval Estimation of the Time in One State to Total Time Ratio in a Double Exponential Process, W. R. Neal (General Electric Co.); *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 361–366; June, 1960.

The exponential distribution is frequently used in the estimation of waiting times and consequently in the mean expected time to failure of a large electronic system. If the repair times following breakdowns are also assumed to be exponentially distributed, a double exponential stochastic process results. The distribution of the observable "uptime ratio" is derived in terms of the eventual expected values as a parameter, and the maximum likelihood estimate of the parameter and the cumulative sampling distribution as a polynomial are obtained.

1105
On the Automatic Detection of Scaling Errors in an Ordvac-Type Arithmetical Organ, G. W. Reitwiesner (Aberdeen Proving Ground); *U. S. Govt. Res. Repts.*, vol. 33, pp. 534–535 (A), May 13, 1960; PB 144 653 (order from LC Mi$2.70, Ph$4.80).

In preparing programming for the solution of problems by fixed radix calculating machines, programmers must scale the arithmetic to satisfy certain number-size restrictions which exist inherently in the functioning of the machines. In complicated problems this may not always be possible, and considerations of machine solution time may prohibit resort to programmed floating radix operation. A very definite advantage accrues when circuits are incorporated into the machine to recognize unanticipated violations of these restrictions and to effect appropriate alarm action when they occur. The design of such circuits is discussed.

1106
Instrumentation for Complex Signal Environment Testing, D. Krueger and G. Herlt, Jr. (HRB-Singer, Inc.); IRE Trans. on Instrumentation, vol. I–9, pp. 13–18; June, 1960.

A simulation program and the equipment developed to facilitate the environmental testing of new receiver, data processing, and display systems without costly, tim consuming field tests are described. T simulator system permits simulation of hig density signal areas, complex pulse-ty modulations, and the effects of bandwid suppression when magnetic tape record are employed.

1107
The Economics of Test Packages, M. Dean (Sperry Gyroscope Co.); IRE Tra on Instrumentation, vol. I-9 , pp. 19–2 June, 1960.

The high costs of testing for reliabil are a deterrent to adequate reliability testi efforts in development programs. Because the enormous sample times required, co ponent (part) testing on the project level usually prohibitive. A method called "t packages" which, when combined with a quate part qualification testing, will yi valuable reliability data at a substantia lower cost is proposed. This method is pa ticularly well suited for computers and oth devices with repetitive assemblies. Furth more, this method yields data based on a tual circuit use of the parts.

1108
Statistical Error Analysis of a Fire Cont Digital Computer, L. H. Chapin (Min apolis-Honeywell Regulator Co.) and I. Whiteman and W. Dixon (General Analy Corp.); *Proc. Fifth Natl. Symp. on R ability and Quality Control in Electroni* pp. 224–229; January 12–14, 1959.

An error analysis of a complex fire co trol digital computer is presented. Throu the use of a statistically designed expe ment, a measure of the performance of t system is obtained with what is felt to b reasonable computational effort. The fr tional factorial experiment used permits c culation of first order effects of the inp parameter perturbations on the outp functions, and an estimate of the interacti effects. These effects are further combi to provide an over-all estimate of the stan ard deviation of each output functi Statistical design applied to planning a n merical analysis is shown to increase t information obtained and to reduce the m nitude of the analysis required.

D-5: PROGRAMS—APPLICATIONS ANALOG COMPUTERS

1109
On the Determination of Certain Errors Analog Computers, N. L. Sosenskii (M cow); *Automation and Remote Control*, v 20, pp. 1349–1358; October, 1959

The effect of the nonlinearity of the f quency characteristics of analog compu operational elements in the solution linear differential equations with consta coefficients is discussed. A graphico-analy method based on the logarithmic frequen characteristics is employed to determine t solution errors. An example of the deter nation of the error in solving a second-or equation is given for the case in which t operational amplifier has a frequen characteristic of complicated form and p sesses a number of parasitic elements.

110
e Simulation of Transfer Functions on Analogue Computer, F. C. Harbert ewis Newmark Ltd.); *Electronic Eng.*, vol. , pp. 354–355; June, 1960.

A one-amplifier circuit for performing e operation of double integration in an alog computer and a method for synthesizg polynomial transfer functions on an alog computer are described. The method general requires fewer amplifiers than the mulation method, which converts the nsfer function to its differential equation rm and sets up the computer to solve this fferential equation. Simulating circuits for ree transfer functions are presented.

E-1: MATHEMATICS—LOGIC, THEORETICAL MATHEMATICS

111
ne Shortest Path Through a Maze, E. F. oore (Bell Telephone Labs.); *Annals of Computation Laboratory*, Harvard Unirsity Press, Cambridge, Mass., vol. 30, . 285–292; 1959.

Several algorithms for finding the shortt path through a maze are presented. The sic algorithm consists of dividing the aze into convenient blocks, writing 0 to rrespond to the beginning of the maze, 1 r each bloc one step from the beginning d so on, until the end is reached. Retracing ck from the end, each step of the retrace ing obtained by going to an adjacent block hose label is diminished by unity, will eld the shortest path through the maze. he algorithm may be modified by assigng the labeling numbers values modulo $n \geq 3$, or by assigning costs to each step. Many applications in communications and ansport problems are suggested.

112
ets-Logics-Machines, G. Kurepa (Inst. Math. Zagreb, Yugoslavia); *Annals of the omputation Laboratory*, Harvard Univerty Press, Cambridge, Mass., vol. 29, pp. 37–146; 1959.

The interconnections among sets, logics nd machines are presented and the fundaental role played by the concept of relaon in establishing such connections is emonstrated. A machine is defined as an put-output or ino-structure. A fundaental problem is that of deciding whether vo ino-structures are functionally equivant.

E-2: MATHEMATICS—LOGIC—SYMBOLIC LOGIC, BOOLEAN ALGEBRA, NUMBER SYSTEMS

113
ogical and Other Kinds of Independence, . Kjellberg (Telefonaktiebolaget L. M. ricsson, Stockholm); *Annals of the Computation Laboratory*, Harvard University Press, ambridge, Mass., vol. 29, pp. 117–124; 959.

Necessary and sufficient conditions for e logical independence of a set of binary ariables are proved. The results are exnded to many-valued variables. Analogies nong logical, stochastic and functional inpendence are presented, and several theotical results are proved.

1114
Some Uses of Truth Tables, T. Singer (Datamatic Corp.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 125–133; 1959.

Various chart manifestations of logical truth tables used by circuit designers are presented. A complete set of truth tables corresponding to the partition of the input variables into pairs of subsets is called a decomposition chart. The practical uses of such charts for determining symmetry and decomposability and for synthesizing functions are described.

1115
Synthesis of a Communication Net, R. T. Chien (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 311–320; July, 1960.

A systematic method for the realization of communication nets from their terminal capacity matrices is given. It is shown that this procedure results in a net whose total branch capacity is minimum for all nets satisfying the same terminal capacity matrix. It is also shown that when the terminal capacity matrix is indeterminate then, for a given total branch capacity, the total terminal capacity is highest when all terminal capacities are made equal.

1116
Some Aspects of Switching Algebra, R. A. Higonnet (Graphic Arts Res. Foundation, Inc.) and R. A. Gréca (Photon:Lumityke, France); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 281–284; 1959.

Suggestions for classifying sequential switching circuits in a manner analogous to combinatorial circuits are made. The number of distinct types of sequential circuits that may be constructed with n relays ($n \leq 4$) are determined. Criteria for eliminating improperly operating circuits are provided.

1117
Symmetric Polynomials in Boolean Algebra, S. Seshu (Syracuse University) and F. E. Hohn (University of Illinois); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 225–234; 1959.

The basic algebra of switching theory is reviewed and the theory of symmetric polynomials in Boolean algebra is developed. It is shown that the set $V_n(Y)$ of symmetric polynomials is a vector space of $(n+1)$ dimensions over the finite Boolean ring B of 2^p elements. The same net $V_n(Y)$ is also a vector space of $p(n+1)$ dimensions over the Boolean ring of two elements 0, 1, which is a subring of B.

1118
Matrix Methods in the Theory of Switching, W. L. Semon (Harvard University); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 13–50; 1959.

The basic results of the theory of switching are developed using a matrix representation. Matrix methods are shown to be particularly valuable in the case of bridge networks, for which the Boolean algebra approach is inadequate. A technique for detecting redundant switches is presented, and a theoretical solution of the problem of finding a minimum circuit for an arbitrary function is indicated.

1119
Multiple-Output Relay Switching Circuits, P. Calingaert (Harvard University); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 59–73; 1959.

A method of reducing the problem of synthesizing switching functions of n variables to one function of $(n+r)$ variables is presented. Given the r functions defined by

$$F_j = \sum_{i=0}^{\nu-1} f_{ji} p_i(x),$$

the single function A defined as

$$A = \sum_{j=i}^{r} F_j \sum_{i=0}^{\nu-1} f_{ji} p_i(x)$$

is formed as the function of the n independent variables and the artificial variables F_j. Once a suitable circuit for A is found, purely formal manipulations provide a multiple-output circuit for the original functions. Questions of minimality and the restrictions placed on the circuit for A are discussed.

1120
The Decomposition of Switching Functions, R. L. Ashenhurst (Harvard University); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 74–116; 1959.

A chart method for the recognition of the disjunctive decompositions of switching functions, together with its theoretical justification, is presented. Extensions to nondisjunctive and more complex types of disjunction are suggested and the algebraic structure of simple disjunctions is developed. Various applications of the decomposition charts, such as finding the prime implicants of a function, with or without "don't care" combinations, are indicated.

1121
Synthesis of Switching Functions By Linear Graph Theory, W. Mayeda (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 321–328; July, 1960.

Techniques of linear graph theory are applied to the study of switching networks. The relationships among paths and circuits in a graph which will give a simple method of analyzing switching networks are considered, and the necessary conditions for the realizability of switching networks consisting of the specified elements are given. The synthesis which is accomplished by the use of the decomposition of cut-set matrices is also discussed.

1122
Algebraic Topological Methods in Synthesis, J. P. Roth (IBM Corp.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 57–73; 1959.

A topological approach to finding a minimum covering set of subcubes for a switching function is developed. A local extraction algorithm that does not require

the examination of all prime implicants considerably reduces the computational labor required, and thus provides a practical solution for considerably more variables than would otherwise be possible.

1123
A Theory of Asynchronous Circuits, D. E. Muller and W. S. Bartky (University of Illinois); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 204–243; 1959.

A complete theory of asynchronous circuits which takes account of possible "race" conditions, time independent circuits and ultimate behavior of circuits is developed. Asynchronous circuits are treated as finite state sequential machines, and many theoretical results linking input and output states are proved.

1124
Remarks on the Design of Sequential Circuits, M. Rubinoff (University of Pennsylvania); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 241–280; 1959.

The design of sequential machines and circuits is approached from the Turing machine viewpoint. The work of Mealy and Moore on merging the states of such a machine is reviewed. A generalized model for sequential machines is presented and a descriptive apparatus of command graphs, dispatcher tables and associated matrices is developed to assist in the design of sequential circuits.

1125
The Application of Graph Theory to the Synthesis of Contact Networks, R. Gould (Harvard University); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 244–292; 1959.

The basic theoretical results of graph theory are presented, and their applications to the theory of switching are described. The methods developed are particularly advantageous for the analysis and synthesis of bridge contact networks, for which Boolean algebra provides an inadequate model. The principle involved is one of mapping a given switching function onto a graph function and then constructing the corresponding graph.

1126
A Mathematical Theory for the Synthesis of Contact Networks With One Input and *K* Outputs, G. N. Povarov (Acad. of Sci. of the USSR); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 74–94; 1959.

A systematic method, known as the method of cascades, whereby the contacts associated with each variable are provided separately for the synthesis of multiple output contact networks is developed and upper bounds for the number of contacts required are derived. The synthesis of symmetric and quasi-symmetric functions is also discussed. Many important theoretical results and upper bounds are provided.

1127
2N-Terminal Contact Networks, F. E. Hohn (University of Illinois); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., pp. 51–58; 1959.

The factoring of the transmission matrix of a switching function into a product of transmission matrices is presented as an important tool for the design of multiterminal as well as two terminal contact networks. Where repetitive patterns occur in the transmission matrix, the method often leads to a series of networks of a limited number of types. This suggests the possiblity of constructing extensive circuits by cascading circuits of simple standard types.

1128
A Survey of Research in the Theory of Relay Networks in the USSR, M. A. Gavrilov (Inst. of Automatics and Remote Control); *Annals of Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 26–53, 1959.

The state of the art in research into the theory of relay contact networks in the USSR is presented. Topics include the analysis of loop and cut sets, special purpose devices for the analysis of relay networks, and the synthesis of single and multiple output networks. The theoretical work of Povarov, Roginski, Lunts and the author is summarized and the direction of further research is outlined.

1129
Applications of Boolean Matrices to the Analysis of Flow Diagrams, R. T. Prosser (M.I.T. Lincoln Lab.); *Proc. EJCC*, pp. 133–138; December 1–3, 1959.

The analysis of the structure of computing machine flow diagrams in terms of Boolean matrices is discussed. A pair of Boolean matrices is associated with each diagram. The first of these, called the connectivity matrix, contains the topological structure of the diagram and the second, called the precedence matrix, contains its precedence relations. Elementary computations on these matrices are shown to yield detailed information concerning the internal logical consistency of the flow diagram. A third matrix, the dominance matrix, which is determined by the connectivity matrix and can be produced from it by a suitable scanning procedure is also considered. Possible applications to automatic debugging procedures are suggested.

1130
An Algebra for Periodically Time-Varying Linear Binary Sequence Transducers, D. A. Huffman (M.I.T.); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 29, pp. 189–203; 1959.

An algebra for time-varying linear binary sequence transducers is developed in terms of the unit delay operator D, and a periodically time-varying operator C. It is shown that a transfer ratio of input to output may be derived in terms of D and C. Means of synthesizing complicated networks from simpler ones, of providing inverse networks, and of minimizing the number of C-elements are discussed.

1131
The Determination of Carry Propagatio Length for Binary Addition, G. W. Rei wiesner (Aberdeen Proving Ground); IR Trans. on Electronic Computers, vo EC-9, pp. 35–38; March, 1960.

It is well known that the expected max mum length of nonzero carry propagation i the addition of two uniformly distribute binary numbers of n-digits each of which less than $\log_2 n$. The propagation of bot zero and nonzero carry is required in the em ployment of asynchronous self-timing add tion. For the addition of two n-digit binar numbers which are uniformly distributed, simple recursive algorithm is readily derive for the exact determination of the ex pected maximum length of zero or nonzer carry propagation.

1132
Conversion Between Floating Point Repre sensations, C. Perry (Stanford Res. Inst.) *Commun. Assoc. for Comp. Mach.*, vol. p. 352; June, 1960.

A process to obtain a compact code fo converting floating point subroutines fro one base to another is described. The con version rests on a formula which is th product of a function of small arguments an range (easily approximated by a low degre polynomial) and another easily compute function.

E-3: MATHEMATICS—LOGIC, NUMERICAL ANALYSIS

1133
A Short Method for Measuring Error in Least-Square Power Series, S. M. Robin son and G. W. Struble (University of Wis consin); *Commun. Assoc. for Comp. Mach.* vol. 3, p. 351; June, 1960.

A method of obtaining a measure of th total error in a least-squares curve fittin process is described. The method makes us of squares already computed and does no require every data point to be stored i memory or a second run through th machine, which are typical disadvantages o alternative methods.

1134
Divisionless Computation of Square Root Through Continued Squaring, D. Sara fyan (University of Florida); *Commun Assoc. for Comp. Mach.*, vol. 3, pp. 319–321 May, 1960.

A divisionless method for extractin square roots, based on the recurrence rela tion $x_{i+1}=(x_i^2/m)+(a/m)$, is described. Re peated use of the recurrence relation yields sieries of approximations to $\sqrt{n}$, wher $n=m^2-4a$. By choosing $m^2\approx n$, rapid con vergence is obtained. To avoid division table of reciprocals of convenient values o m is stored. Convergence is assured if th starting value x_0 is chosen to lie within th interval $(-m/2, m/2)$. A satisfactory choic is $x_0=a/m$.

1135
Householder's Method for the Solution o of the Algebraic Eigenproblem, J. H Wilkinson (Natl. Physical Lab.); *Compute J.*, vol. 3, pp. 23–27; April, 1960.

A practical method for the solution of eigenvalue problem, based on a method Householder, is described. The House-ler method reduces a symmetric matrix ridiagonal form by means of a similarity nsformation, the orthogonal matrix of ch is obtained by the multiplication of ple orthogonal matrices which are not ie rotations, in contrast to the methods Lanzos and Givens. The method is med to be the most satisfactory of wn methods for symmetric matrices and y have considerable advantages for non nmetric matrices. Details are illustrated means of a simple example.

E-5: MATHEMATICS—LOGIC, INFORMATION THEORY

6

ies for the Correction of "Clustered" ors, S. H. Reiger (RAND Corp.); IRE ANS. ON INFORMATION THEORY, vol. IT-6, 16–21; March, 1960.

A method which permits the systematic struction of codes capable of error-free nsmission, provided errors occur in usters" of limited duration, is described. e method is valid for error clusters of any scribed duration. The codes are rela-ely easy to implement and decoding erations are straightforward. Specific mples are given and applications to etype transmission are discussed.

7

or Correcting Codes for Correcting rsts of Errors, J. E. Meggitt (IBM rp.); *IBM J. Res. & Dev.*, vol. 4, pp. 329–4; July, 1960.

It is observed that the codes of Abram-n, Melas and others are essentially de-ibed by the characteristic equation that a tain matrix satisfies. Consequently it is nd that transformations of these codes possible provided the characteristic uation is preserved. These transforma-ns may then be exploited to produce les that have a simple implementation. general method is indicated by which any le may be implemented when the charac-istic equation is known.

38

Note of P-Nary Adjacent-Error-Correct-g Codes, B. Elspas (Stanford Res. st.); IRE TRANS. ON INFORMATION EORY, vol. IT-6, pp. 13–15; March, 1960.

The generalization of Abramson's binary up codes for the correction for all single ors and all double errors in adjacent digits the p-nary case, where a symbol alphabet nsisting of the digits 0, 1, . . . , p-1 is used transmission, p being a prime number, is cussed. Examples of such p-nary codes given, as well as necessary conditions for ir existence. These codes bear the same ation to the p-nary Golay codes as ramson's codes do to the familiar Ham-ming codes. Some as yet unanswered questions are raised, and suggestions for further possible generalizations are given.

E-6: MATHEMATICS—LOGIC, LINEAR PROGRAMMING

1139

Simultaneous Equations and Linear Programming, K. T. Boyd (Unilever Ltd., London); *Computer J.*, vol. 3, pp. 45–46; April, 1960.

A modification of the well-known Simplex method for linear programming that produces, in one run, the solution of a set of simultaneous linear equations and the inverse of the matrix of coefficients is described. The non-negativity rule usual in linear programming places no restriction on the problems that can be considered. The method can also be used for the inversion of matrices not associated with simultaneous equations.

1140

The Logical Design of Electrical Networks Using Linear Programming Methods, U. G. W. Knight (Merseyside and North Wales Electricity Board); *Proc. IEE*, vol. 107, pt. A, pp. 306–313; June, 1960.

The results of an investigation into the mathematical design, as distinct from analysis, of electrical power-system networks are described. Starting with the geographical positions of the substations which it is required to interconnect, it is shown that a set of equations can be obtained which are solvable by linear-programming techniques to provide a minimum-cost network design. Any degree of security of supply conditions considered necessary can be incorporated into the design equations. Solution of the resulting linear programs requires the use of a digital computer; the necessary computer size and amount of computation increase rapidly with increase in the number of substations to be incorporated. With this in mind, suggestions for increasing the size of problem solvable on a given computer are made. Three designs have been completed using the method proposed. These and the results of network-analyser studies on two of them are summarized. The equations for two other possible network-design criteria, i.e. minimum circuit length and minimum apparent-power by distance product, are also given and briefly commented upon.

1141

On the Job-Shop Scheduling Problem, A. S. Manne (Yale University); *Operations Res.*, vol. 8, pp. 219–223; March–April, 1960.

The application of discrete linear programming to the typical job-shop scheduling problem—one that involves both sequencing restrictions and also noninterference constraints for individual pieces of equipment—is proposed. Thus far, no attempt has been made to establish the computational feasibility of the approach in the case of large-scale realistic problems. This formulation seems, however, to involve considerably fewer variables than two other recent proposals, and on these grounds may be worth some computer experimentation.

J: SUMMARIES AND REVIEWS

1142

The Future of Automatic Digital Computers, A. D. Booth; *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 339–341; June, 1960.

Most of the latest developments in computing design and programming, such as parallel processing, microsecond operations, time-sharing, and microprogramming are shown to have their origin in the earlier work of groups such as that at Princeton under the late J. von Neumann. Future advances are to be expected from improved semiconductor devices, magnetic films, cryotrons and improved input-output mechanisms.

1143

The Department of Computer Mathematics at Moscow State University, L. S. Berezin (Moscow State University); *Commun. Assoc. for Comp. Mach.*, vol. 3, pp. 342-344; June, 1960.

The organization and teaching curricula of the newly organized Department of Computer Mathematics at Moscow University are summarized. The curriculum is divided into basic courses, seminars, and laboratory exercises. A five-year diploma program is offered. A high-speed STRELA computer is available.

1144

Switching Research in Germany, A. Walther (Darmstadt, Germany); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 295–301; 1959.

The state of switching research in Germany through 1957 is reviewed. The work of three manufacturers and four universities is referred to. The main topics are matrix operations in switching theory and magnetic core logic.

1145

Switching Research in Spain, J. G. Santesmases (University of Madrid); *Annals of the Computation Laboratory*, Harvard University Press, Cambridge, Mass., vol. 30, pp. 99–114; 1959.

The development of switching research in Spain, from the early work of Torres-Quevodo in the 1890's to the present, is traced. Present work is mainly concerned with the development of ferroresonant flip-flops and switching elements. The basic configuration is one in which a core and a capacitor are placed either in series or in parallel.

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PGEC News

OBITUARY

HARRY H. GOODE

Harry H. Goode (SM'52), Professor of Electrical Engineering at the University of Michigan, Chairman of the National Joint Computer Committee, and a prominent leader in the activities of the PGEC, died in an automobile accident on the morning of October 30, 1960. His loss will be deeply felt by all who knew him through his teaching, his frequent lecture appearances, his many publications, his work in professional societies, his consulting activities, his stimulating participation in conferences, or directly through his warm friendship.

Prof. Goode was born in New York, N. Y., on July 1, 1909. He received the B.S. degree in history from New York University in 1931, and later earned the Bachelor of Chemical Engineering degree from Cooper Union in 1940 and the M.A. degree in mathematics from Columbia University in 1945. His early professional work was in statistics, and in 1941 he became Statistician-in-Charge for the New York City Department of Health. During the war years he was a research associate at Tufts College and worked on applications of probability to war problems and also on the acoustic torpedo problem. From 1946 through 1949 he was on the staff of the Office of Naval Research at the Special Devices Center, Sands Point, Long Island. Here he progressed through successive responsibilities to be head of the Special Projects Branch. His work during this period was on flight control simulation and training, aircraft instrumentation, antisubmarine warfare, weapons system design, and computer research. Through his ONR work he participated in such pioneer computer projects as the Whirlwind computer at M.I.T., the Cyclone computer built by Reeves Instrument Company, in New York, and the Typhoon computer built by RCA Laboratories for the Navy.

In 1950 he joined the Willow Run Research Center of the University of Michigan, serving there first as head of the Systems Analysis and Simulation Group, then as Chief Project Engineer, and ultimately as Director of the Center. Under his direction the Research Center carried forward a broad program of research, including computers, system design, radar, infrared, and acoustics. He guided the efforts of the Center through problems in air defense and battle area surveillance and was instrumental in the successful completion of the ground system for the Bomarc missile.

In 1954 he was appointed Professor of Electrical Engineering at the University of Michigan, and in 1956 his wide range of interests brought a dual appointment as Professor of Electrical Engineering and also as Professor of Industrial Engineering. In 1958 he served for a year as Technical Director of the Systems Division of the Bendix Corporation, maintaining a fractional appointment in the University so that he could continue to teach his newly introduced course on System Design. A little over a year ago he returned to full-time teaching and research activities in the Department of Electrical Engineering.

In addition to his wide range of services to the University of Michigan, Professor Goode also served as a consultant to industry and government and was active in professional society affairs. He brought to problems a keen insight and a rare ability for stripping away the nonessentials. His advice was highly valued and widely sought. Among the firms for which he consulted were the United Aircraft Corporation, the Bendix Corporation, the Auerbach Electronics Corporation, the DuPont Corporation, the Ford Motor Company, the Burroughs Corporation, the Texas Company, and the Franklin Institute. He served the government as a consultant to the National Bureau of Standards, the Post Office Department, the Air Force, and the House of Representatives Appropriations Committee. For the Air Force, he was chairman of the W-117L Committee on Advanced Reconnaissance; and for the House Committee, he served as a member of the Study Group on Missile Reliability.

He served his profession as a member of the Administrative Committee of PGEC from 1953 to 1956, as a member of the Computer Advisory Committee of the Society of Automotive Engineers, and as a member of a subcommittee of the AIEE Committee on Feedback Controls. His most important service in this area was as chairman of the National Joint Computer Committee of IRE, AIEE, and ACM. He played an important part in the formulation of the charter under which these three organizations will join to form the new American Federation of Information Processing Societies, which in turn will represent this country in the Internation Federation of Information Processing Societies.

Professor Goode was a Fellow of the American Association for the Advancement of Science, and a member of the Association for Computing Machinery, the American Mathematical Society, the Mathematical Association of America, the Institute for Mathematical Statistics, Sigma Xi, Eta Kappa Nu, and Mu Alpha Omicron.

His many published papers touched upon statistics, simulation and modeling, vehicular traffic control, and system design. His major published work is the book "System Engineering," of which he was senior author with R. E. Machol. The book was the outgrowth of the very successful and valuable course which he introduced at the University of Michigan under the title, "Large Scale System Design."

Professor Goode's broad experience with computers and his participation in national computer functions led to his participation as one of the group of eight Americans who visited Soviet computer establishments in 1959.

Our profession has lost one of its most outstanding members—a man of rare versatility, talent, vigor, and vision.

—On behalf of PGEC, the Editor wishes to thank Professor Norman H. Scott of the University of Michigan for providing the foregoing appreciation of the late Harry H. Goode.

ADMINISTRATIVE COMMITTEE MEETS

On December 12, almost simultaneous with the appearance of this issue, the PGEC Administrative Committee will be meeting in New York, just prior to the EJCC. The agenda includes further consideration of the role of AFIPS, the proposed American Federation of Information Processing Societies, and normal business such as budgets, etc.

To All PGEC Chapter Officers

The PGEC *News* page of these TRANSACTIONS is open for your announcements and report of activities. Deadline is the first of the month, two months ahead of the date of the issue. Send all items to the *Editor*.

Notices

COMING MEETINGS

1960 EASTERN JOINT COMPUTER CONFERENCE

The tenth IRE-AIEE-ACM Eastern Joint Computer Conference will be held December 13–15 at the Hotel New Yorker and the Manhattan Center in New York,

Abstracts of the papers to be presented are given below.

I. Tuesday: December 13—9:30–11:40 A.M.

I.0. Opening Remarks: N. Rochester, *Conference Chairman,* IBM Corp., and E. C. Kubie, *Program Chairman,* Computer Usage Co.

I.1. A Logical Machine for Measuring Problem-Solving Ability, C. R. Langmuir—The Psychological Corp.

The magnitude of costs incurred by assigning unsuccessful or even marginal personnel to tasks involving EDP systems design and programming justifies a much greater effort in the selection of personnel than the use of conventional aptitude tests implies. A small desk-top machine named the Logical Analysis Device is described, its logical organization is explained, and its operation as a method of observing and testing an individual's problem-solving abilities is illustrated with slides. Some comment describing the wide variation of performance among several hundred college graduates employed in various professions is included, but the principal emphasis is given to data pertaining to the performance characteristics of persons in computer and data processing activities.

The application of the device is clearly indicated at the point of evaluating final candidates for assignment to tasks requiring a high order of logical and analytical talent.

I.2. A Method of Voice Communication With a Digital Computer, S. R. Petrick and H. M. Willett—AF Cambridge Res. Labs.

A pattern recognition procedure for achieving automatic recognition of spoken words has been developed and instrumented using an eighteen-channel vocoder and a general-purpose medium scale computer. If the speaker's own voice is used to prepare "masks" of the words he wishes to be recognized, correct identifications are made and printed on the computer flexowriter with almost 100 per cent accuracy. Arbitrary new spoken input words may be added in real time to the computer vocabulary. Other programs dependent upon this word recognition facility which have been written include:

1) An interpretive routine which enables a speaker to say a sequence of words (from the set zero, one, . . . , nine, plus, minus, times, bracket, equals) which are followed by a print out of the words spoken and the value of the expression defined.
2) A speaker recognition program which identifies the talker with appropriate comments as well as the word he spoke.
3) An adaptive program which enables the computer to reorient itself automatically to a new speaker's voice.

I.3. FILTER—A Topological Pattern Separation Computer Program, D. Innes—Lawrence Radiation Lab.

The advent of high energy particle accelerators and liquid bubble chamber detectors has added the demands of high-speed data reduction to the many problems of modern nuclear physics research. For example, one six-month experiment on the University of California's 72-inch Hydrogen Bubble Chamber yields photographic records of millions of nuclear events. This paper discusses one of the new measuring and topological identification devices which has been developed to analyze these great volumes of research data.

Dr. Bruce McCormick has proposed a scanning technique which allows rapid recognition, separation and measurement of the photographic records of star-type nuclear events. A device known as the Spiral Reader measures background and star-type event features, impartially discriminating against nonradial patterns by the geometry of its rotating scanning element. The event measurements are separated from the background measurements by an IBM 709 computer under the direction of a program called FILTER. The separated nuclear event measurements are subsequently reconstructed in space for physics analysis.

FILTER exploits the observation that if a segment of a circular arc is rotated about a point on that arc, intercepts occur at regular intervals along a radius to the point at constant angular intervals of the rotation azimuth. The Spiral Reader, by placing the burden of event discrimination on a high-speed digital computer, minimizes the need for either special analysis equipment or for a human operator to make the topological separation. Simulation, calibration and cathode-ray-tube display routines have been included in the FILTER system. A description of the Spiral Reader and FILTER program will be followed by several examples of the program's ability to separate and measure these star pattern nuclear events.

I.4. Redundancy Exploitation in the Computer Solution of Double-Crostics, E. S. Spiegelthal—Consultant.

There are many data-processing applications for which exact algorithmic processing schemes are either not strictly required or defy precise specification or both. Such applications as machine translation, automatic abstracting and automatic indexing fall in this category. The human beings who execute these tasks make heavy use of the redundancy of the input data. What is required for their automation is some heuristic scheme for taking advantage of this redundancy. One such scheme is described in the present paper. This scheme, in its first concrete realization, has been used to solve Double-Crostic puzzles. Both the 704 programs for Double-Crostic solution and the general heuristic scheme are discussed in the paper.

II. Tuesday: December 13—2:00–4:05 P.M.

II.1. A Computer for Weather Data Acquisition, P. Meissner, J. Cunningham, and C. Kettering—National Bureau of Standards

In order to meet a growing need for more rapid and detailed reporting of weather information, the U. S. Weather Bureau has been conducting an extensive program for the development of automatic weather stations. The National Bureau of Standards has had an opportunity to participate in this program and has developed a small specialized computer for use as the control component in such a station. The computer is intended as a research tool for exploring the application of automatic data processing equipment to this type of problem. Basically, the computer must sample a number of weather-sensing instruments, suitably process the instrument data, and prepare outputs in the form of local displays and teletype messages. Since the machine is internally programmed, it will afford a wide latitude in the processing of input data including the simultaneous comparison of results obtained in different ways.

The design of a computer for this application was felt to be justified on the basis of a number of special requirements. Among these are:

1) Parallel inputs from a number of separate sources,
2) Multiple outputs in several forms,
3) Concurrent operation of input, output, and data processing functions,
4) Extensive reference tables with special instructions for their use,
5) Limited arithmetic capability,
6) Three-digit word length,
7) Computing speed need not be high.

II.2. A Survey of Digital Methods For Radar Data Processing, F. H. Krantz and W. D. Murray—Burroughs Corp.

This paper reviews the growing number of declassified techniques for automatic processing of radar data by digital means. Emphasis is placed upon signal time-sampling and quantization, integration methods, rejection of stationary targets, radar trigger manipulation, and a new high-speed device for recording digitized radar video. These techniques are discussed individually and are also shown combined in a hypothetical radar data processor design.

I.3. The Organization and Program of the BMEWS Checkout Data Processor, A. Eugene Miller—Auerbach Electronics Corp., and M. Goldman—RCA.

The BMEWS Checkout Data Processor (CDP) is probably the first medium-size digital processor to perform the real-time, on-line checkout of an entire operational radar detection and processing system. This paper is the first to discuss publicly the unique organization of the BMEWS CDP and the unusual structure of its program. The CDP is one of the major subsystems of the Ballistic Missile Early Warning System.

The CDP has separate memories; one for storing constants and instructions, and one for storing data. The means for jointly using these two different types of memories, while maintaining the flexibility associated with single memory machines, is explained. The tailored features of the CDP, efficiently handling its unique problems, are emphasized. They include real-time program interrupt signals and a complex input-output system. This input-output system, as well as communicating with over a dozen other digital data handling devices, has more than 250 separate addresses.

The discussion of the complex structure of the CDP program covers the three separate programs which run in an interwoven fashion. It describes the solution of problems caused by this interweaving and by the real time program interrupt.

I.4. Ultra-High-Speed Dynamic Display System for Digital Data, B. G. Tregub—Melpar, Inc.

A new ultra-high-speed direct-view cathode-ray tube presentation of digital input data is described. This system is capable of locating a point anywhere on a 16-inch electrostatic cathode-ray tube within 5 microseconds with an over-all repeatability (including amplifier settling times) of 0.05 per cent. The present system as it exists in production is actually a dual unit which is capable of plotting lines, dots and cursor patterns on the face of the cathode-ray tube as ordered by data blocks on a magnetic drum during 33-μsec intervals. Color displays are also presented by means of the field sequential technique. Input data utilizes 12 bits per point to identify each of the X and Y coordinates for each end of the line. Intensity is controlled by additional binary inputs. The cathode-ray tube operates at 15 kv and the display system includes automatic focusing correction to compensate for deflection defocusing. Spot size is approximately 30 milli-inches with point end line placement accurate to within 20 milli-inches.

I.5. High Speed Data Transmission Systems, R. G. Matteson and J. D. Barnard—Stromberg-Carlson Co.

With the rapid increase in the use of digital computers for business, scientific control, and military applications requirements are created for the high-speed transmission of data so that these computers may be utilized for more and diversified applications, and so that computers may be utilized a greater percentage of the time. This paper will describe areas of application of high-speed data transmission equipment and will describe equipment developed and installed by Stromberg-Carlson for the transmission of digital information over standard telephone lines at 2400 bits per second. One of the units described in detail in the paper is a unique type of magnetic tape transport designed to operate in two modes, a stepping asynchronous mode, or a continuous, synchronous mode.

III. Wednesday: December 14—9:00–11:05 A.M.

III.1. Parallel Computing With Vertical Data, W. Shooman—System Development Corp.

A novel technique called Vertical Data Processing (VDP) for the manipulation of data on digital computers is presented. Multiple data are processed simultaneously one bit at a time using Boolean operations. Several classes of problems appear adaptable to this technique.

A hypothetical VDP computer which embodies both VDP as well as conventional techniques is proposed and its advantages discussed.

III.2. The TABSOL Concept, T. F. Kavanagh—General Electric Co.

This paper describes how Decision Structure Tables can be used to describe complex, sequential, multivariable, multiresult decision systems. TABSOL, an automatic programming technique for solving structure tables on any computer is also discussed.

The structure table and TABSOL concepts are major steps forward in describing complex operating decision systems since they replace both flow charting and computer coding. In addition, changes can be readily introduced by the systems designer, greatly simplifying the systems maintenance problem. By forcing a logical step-by-step analysis, these techniques highlight business causal relationships and simplify debugging in the systems designer's own language.

III.3. Theory of Files, L. Lombardi—University of California, Los Angeles.

The theory of files is a tool for the logico-mathematical treatment of automatic non-numerical data processing problems, such as machine accounting, information retrieval, and mechanical translation of languages. The main result which has been obtained from the application of this theory is the recent discovery of a simple pattern to which the data flow of any information processing procedure conforms, regardless of how many files are involved. The flow of each file can be controlled and coordinated with the flow of the others by means of five Boolean parameters, called *indicators*. A specially designed Algebraic Business Language exploits these results for the purpose of programming digital data processors. This paper also probes into the impact of the theory of files upon the logical design of digital systems.

III.4. Polyphase Merge Sorting—An Advanced Technique, R. L. Gilstad—Minneapolis-Honeywell Regulator Co.

New merge sorting techniques have been developed by Honeywell that utilize tape drives more efficiently than conventional sorting methods. A report on one of these techniques, the Cascade or "N-1" sort, was presented a year ago. A review of the Cascade sorting method is presented in the current paper as background for a new advancement, called polyphase sorting. The methods used in polyphase sorting are explained in terms recognizable by anyone familiar with merge sorting on computers. Arguments are brought forth comparing the merging power of normal merge sorting, Cascade, and polyphase techniques. These arguments show that Cascade sorting and polyphase sorting represent techniques that make the new generation of computers even more powerful than before in one of the most common areas of computer usage.

III.5. The Use of Binary Computers For Data Processing, G. H. Redmond and D. E. Mulvihill—Chrysler Corp.

The paper presents a case concerning the use of binary machines for data processing. Based on experience gained by the Chrysler Corporation, the paper discusses the need for the establishment of a consistency of concept for all phases of problem organization and solution. Specific advantages inherent in binary machines are pointed out, along with some of the pitfalls which would result if the consistency of concept is not maintained. A warning is sounded to those concerned with the development and use of generalized business oriented languages that certain abilities of binary machines have not been exploited in these programs. In conclusion, it is stated that the abilities of binary-type machines will become more indispensable as management techniques extant today become more sophisticated and acceptable.

IV. Wednesday: December 14—2:00–4:30 P.M.

IV.1. High Speed Printer and Plotter, F. T. Innes—Briggs Associates, Inc.

The high-speed printer and plotter is capable of plotting ten simultaneous curves each at a rate of 100 points per second or of printing at a rate of 66 lines per second. Its principal application is in producing annotated plots with grid lines and alphameric annotation.

The machine uses magnetic tape input, hybrid resistor-transistor and diode logic, with a multiple stylus electrolytic recorder for output with paper moving at ten inches per second. Programming general organization and design features will be discussed. Typical annotated plots from the machine will be shown.

IV.2. A Description of the IBM 7074 System, R. R. Bender, D. T. Doody, and P. N. Stoughton—IBM.

The IBM 7074 System, the second major step in the IBM 7070 Data System family, provides increased processing power by improvements within the framework of the 7070. A new circuit card and the IBM Standard Modular System of packaging make possible system growth by substitution of functional units rather than by replacement of an entire system. Program compatibility with the 7070 is retained. Increased proc-

essing speeds are attained by faster circuits, full parallel arithmetic, and the use of faster storage. Circuits, packaging, and machine organization will be described. Examples of instruction execution times will be given and their effect on system performance will be discussed.

IV.3. The RCA 601 System, D. L. Nettleton and K. K. Kozarsky—RCA.

The technical aspects of the RCA 601 are discussed with particular emphasis on the three dimensions of an RCA system which may be readily modified at the user's option—speed, function, and capacity. Design features such as a 1.5-μsec memory, 120-kc tapes, and generalized word structure are also described. Several representative systems are summarized to illustrate the tailoring of RCA 601 systems to such varied applications as payroll, engineering analysis, or file maintenance.

The advances in program logic, which enable the system to take advantage of the fast memory and tapes, an arbitrary degree of simultaneity and the generalized word and character structure, are explored. Emphasis is placed upon variable instruction length, the address modification and listing structure, and parallel or simultaneous processing.

IV.4. Associative Self-Sorting Memory, R. R. Seeber, Jr.—IBM.

A major problem in data processing is the sorting of data. This paper proposes a memory system which automatically performs the sorting function. An associative memory, based on cryotron circuits, is extended to permit high-equal-low comparison of the interrogating word with all words in memory. This comparison permits the new word to be placed between the proper pair of sorted words in the memory. A double shifting operation is used to move the appropriate block of words to make room for the new word.

IV.5. UNIVAC-RANDEX II—Random Access Data Storage System, G. J. Axel—Remington-Rand Univac Div., Sperry-Rand Corp.

A random-access drum file having 198.6 million bits total storage capacity, a bit density of 650 pulses per inch, and 385 msec average data access time is described in this paper.

Two flying-magnetic-recording heads transfer data to and from the drum file unit. They are self-supported, by a hydrodynamically generated air film, over two magnetically plated drums (24 inches diameter and 44 inches long). The heads, drums, and head-positioning servo are enclosed in a sealed and pressurized chamber to prevent their contamination by foreign material normally found in the atmospheric air. The text includes:

1) The logic of operation and a description of the over-all drum file.
2) Construction of the flying-heads.
3) Descriptions of the servo and mechanical adder that positions the flying-heads over selected addresses on the drum.

IV.6. Hot-Wire Anemometer Paper-Tape Reader, J. H. Jory—Soroban Engineering, Inc.

A hot-wire anemometer type reader is proposed as a method of achieving reliable, high-speed reading of perforated paper tape.

The principle of operation concerns the change in resistance of a fine coil of wire of known temperature coefficient of resistance when subjected to an air stream directed through a perforation in a paper tape being read.

V. Thursday: December 15—9:00–11:05 A.M.

V.1. Data Processing Techniques in Design Automation, W. L. Gordon—Minneapolis-Honeywell Regulator Co.

By providing a computer with basic information concerning the design of a device as complex as the modern computer one not only obtains an efficient record retention system but also brings to bear the full decision-making abilities of the computer on the design problem itself. A major thesis of this paper is that the automation of the design of a complex system is primarily a data-processing probelm in which the most powerful tools reside in the ability of the computer to perform such jobs as editing, extracting, sorting, and merging pieces of basic design information. This contention is substantiated by describing the system currently in use to provide mechanized aids to design and production at Minneapolis-Honeywell DATAmatic.

V.2. Impact of Automation On Digital Computer Design, W. A. Hannig and T. L. Mayes—General Electric Co.

The impact of design automation techniques upon the design, construction, and maintenance of digital computers is discussed. Specific items described include:

1) The logician's use of these programs as a design tool.
2) The use of the documents produced by these programs.
3) The effect that the use of these programs and program-produced documents has upon the human organization using them.

This paper further describes the use to which automation programs were put in the design of presently operating digital computers, starting with Boolean-equation input data and ending with factory release information.

V.3. Calculated Waveforms For Tunnel Diode Locked Pair, H. R. Kaupp and D. R. Crosby—RCA.

This paper presents an introductory analysis of the tunnel diode locked-pair circuit. The characteristics of the tunnel diode, together with the simplicity of the locked-pair circuit, make it a major contender for use as a high-speed computer element. High speed and high gain are the locked pair's main advantages; the three-phase power supply and lack of a simple means for logical inversion are its main disadvantages. The basic circuit consists of two tunnel diodes in series, the node common to the tunnel diodes being both the input and output terminal. As a computer element, the locked pair functions in much the same manner as the phase-locking harmonic oscillator (PLO). Like the PLO, the locked pair overcomes the difficulty of coincident input and output terminals by using a three-phase voltage source.

This paper also demonstrates the feasibility of using a digital computer to solve nonlinear circuit prŏblems. A digital computer makes possible an exact solution by doing away with relatively ineffectual linear approximation techniques. Furthermore, the stray parameters associated with laboratory work at high frequencies are excluded, thereby disclosing the true nature of the circuit.

V.4. On Iterative Factorization in Network Analysis By Digital Computer, W. H. Kim, C. V. Freiman, and W. Mayeda—Dept. of Elec. Engrg., Columbia University.

The need to determine the sum of all tree admittance products occurs in almost all applications of topological network theory. This paper describes a method of obtaining this sum through an iterative factorization of the sum of tree admittance products of successively more complex subnetworks. Computational efficiency is achieved in that: 1) it is not necessary to test sets of branches for the presence of circuits; and 2) it is not necessary to calculate each tree admittance product.

A digital computer program has been developed for use on an IBM 704 which accommodates networks of up to 13 nodes and 77 branches. The program is designed to reduce computation time when the present network corresponds to a minor modification of the previously investigated network. Use is made of a lexicographic enumerating function to develop working constants for networks of various size. Estimates of computing time and flow-charts of the program are included, as is a table of the number of unique partitions of an n-element set ($n = 1, 2, \cdots, 12$).

V.5. A Computer-Controlled Dynamic Servo Test System, V. A. Kaiser and J. L. Whittaker—Douglas Aircraft Corp.

A computer-controlled dynamic servo test system has recently been placed in operation by the Testing Division of Douglas Aircraft Corporation. The manual operations normally performed in the testing of a missile control system are now entirely accomplished by this computer installation. In obtaining the frequency response and stability characteristics of a control system, the computer operates to 1) generate a prescribed sequence of driving functions, 2) sample the resulting outputs, 3) compute from these samples the gain and phase characteristics, and 4) provide tabulated or plotted results in a form ready for analysis. This unique application of a general-purpose digital computer will vastly reduce the time required in the development of missile control systems, subsystems, and components. A description of the equipment used and the analytical techniques em-

ployed to enable automatic dynamic testing is given. A comparison of the time required and accuracy obtained using this new automatic facility with that of the conventional manual method of servo testing is presented.

VI. Thursday: December 15—2:00–4:05 P.M.

VI.1. The Flying Spot Scanner As An Input Sensor To A Character Reading System, J. S. Bryan, J. B. Chatten, F. P. Keiper, and C. F. Teacher—Philco Corp.

It is shown that the Flying Spot Scanner meets most of the requirements of an ideal sensor for a character recognizer. Advanced electron optics and phosphor technology now make practical the all-electronic scanning of an entire page of printed material. The signal-to-noise ratio is such that picture element errors due to the quantum fluctuations at the photocathode have the probability of occurrence of only 2.5×10^{-7} when the video bandwidth is 6 Mc and the CRT beam current is sufficiently low to insure good tube life. Techniques are presented which minimize spacial quantization errors that are inherent in conventional scanning procedures. Other techniques are discussed which increase the readability of degraded printing for a recognizer.

VI.2. Use of A Digital/Analog Arithmetic Unit Within A Digital Computer, D. Wortzman—Advanced Systems Dev. Div., IBM.

This report discusses the use of a Digital/Analog Arithmetic Unit in order to increase the computational power of digital computers. In some problems the inherent high accuracy of digital computers is unwarranted either because the input digital information is limited in accuracy or because the input information is in analog form. It is in these instances that the Digital/Analog Arithmetic Unit's high speed, ease of programming, and ability to operate on combined analog and digital information may be welcomed.

VI.3. PB250, A High Speed Serial General-Purpose Digital Computer Using Magnetostrictive Delay Line Storage, R. M. Beck—Packard Bell Computer Corp.

The requirements for a small general-purpose computer that can serve as a system component as well as a general computing device are described, together with an analysis of alternate methods of mechanization. The PB250 is then described and evaluated as an optimum solution to these requirements. Methods for minimizing active elements and logical devices that serve to increase flexibility are described in detail.

VI.4. The Instruction Unit of the STRETCH Computer, R. T. Blosk—IBM.

The Instruction unit, which is a large, complex, high-speed computer, is designed and built to provide the major function and control ability for the STRETCH Computer. The purposes of this paper are to describe the major functions of the unit, to give a general picture of the internal machine organization, and to present several examples of how some performance goals are achieved The Instruction unit has a variety of functions. Most important are the fetching and indexing of all instructions for the computer, and the execution of a large set of instructions dealing with index arithmetic, branching, and word transmission. The size and complexity of the unit are determined by the instruction buffering and the extensive amount of simultaneous operations required to achieve the high performance goals set for the computer.

VI.5. The Printed Motor: A New Approach To Intermittent and Continuous Motion Devices in Data-Processing Equipment, R. P. Burr—Circuit Research Co.

The printed dc motor is characterized by high pulse torque capability and freedom from cogging or preferred armature positions. These attributes lead to a variety of applications in data processing equipment ranging from reel and capstan drives in magnetic and paper tape transports through detenting and positioning mechanisms. Analysis of the motor on a velocity basis yields a simple equivalent circuit which is a powerful tool for designing both the machine and its drive circuits into a specific requirement. Since there is no rotating iron in the structure and since the field is supplied by permanent magnets, the speed-torque curve of the motor is a straight line whose slope defines a "mechanical source impedance." Inertia of the proposed load appears as a capacitor in the same dimensional system. When the desired machine motion can be expressed in terms of velocity and the inertia of the load is known, the shape and magnitude of the necessary driving signal together with the power which must be expended can all be determined for the operating cycle. A typical example of an application in a paper tape transport is described.

COMBINED ANALOG-DIGITAL COMPUTER SYSTEMS SYMPOSIUM

Simulation Councils, Inc., and the Missile and Space Vehicle Department of the General Electric Company are sponsoring a symposium on Combined Analog-Digital Computer Systems, to be held on the Friday and Saturday following the EJCC, December 16 and 17, 1960, at the Sheraton Hotel in Philadelphia. At this writing the program has not yet been announced in detail, but the following sessions are planned, all relating to combined systems.

1) Equipment and Design—Dr. Harold Skramstad, *Chairman*
2) Application—George Bekey, *Chairman*
3) Programming—Dr. Marcel Martin, *Chairman*
4) Future Developments—Joseph Pachuta, *Chairman.*

General Chairman for the symposium is Martin Paskman, MSVD, General Electric Co., Philadelphia 4, Pa.

JOINT SIAM—AAAS SESSION

The customary joint session sponsored by the Society for Industrial and Applied Mathematics and the American Association for the Advancement of Science will be held at 9 A.M., December 28, 1960, during the AAAS annual meeting at the Biltmore Hotel in New York. Titles of the session and papers are as follows:

Mathematics Looks at New Problems

Chairman: James H. Griesmer, IBM Research Center.

1) "Applications of Game Theory to Military Strategy and Tactics," D. Gillette, Bell Telephone Laboratories.
2) "An Application of Graph Theory to Group Dynamics," F. Harary, University of Michigan.
3) "The Role of Mathematics in Control Systems," J. E. Bertram, IBM Research Center.

1961 IRE INTERNATIONAL CONVENTION

The next IRE International Convention is scheduled for March 20–23, 1961, at the Coliseum and Waldorf-Astoria Hotel in New York. The deadline for submission of papers is past, and E. C. Johnson, Head of the Computer Development Department of Bendix Corporation, PGEC representative to the Program Committee, is now in the final stages of completing the planning for PGEC's technical sessions at the convention.

1961 IRE-AIEE-U OF P INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

The 1961 International Solid-State Circuits Conference, the 8th annual such meeting, will be held February 15–17, 1961, on the campus of the University of Pennsylvania and at the Sheraton Hotel, Philadelphia, Pa.

The conference, sponsored jointly by the IRE, AIEE, and University of Pennsylvania, will feature papers dealing with circuit properties, circuit philosophy and design techniques related to solid-state devices in the following general areas:

Solid-state memory, storage, and logic elements, such as twistors, thin-film memories and associated circuits, photoelectronic circuitry, etc.

Solid-state microwave amplifying mechanisms, such as parametric amplifiers and masers.

Solid-state devices performing an integrated circuit function.

Cryogenic digital and linear applications.

Novel types of solid-state devices in unique modes of operation such as those utilizing the Hall effect, high-temperature circuit elements, and solid-state filters and delay lines.

Advanced circuitry with emphasis on significant developments in the art, to the exclusion of data on equipment design.

For further information, contact the public relations officer,

Lewis Winner,
152 West 42nd St.
New York 36, N. Y.

1961 WESTERN JOINT COMPUTER CONFERENCE

The annual Western Joint Computer Conference will be held in Los Angeles, Calif., on May 9–11, 1961, at the Ambassador Hotel. Dr. Walter F. Bauer is general chairman. See the CALLS FOR PAPERS below.

CALLS FOR PAPERS

1961 WESTERN JOINT COMPUTER CONFERENCE

The theme of the conference is "Extending Man's Intellect" to emphasize the role that computers have played in scientific, technical, and business advances in recent years.

Technical papers are solicited in the areas of systems, applications, and circuitry for both digital and analog computers. Papers are sought in a wide range of subjects including, for example, papers on large-scale computer systems, thin-film memory devices, cryogenic devices, automaton theory, pattern recognition, automatic programming, medical uses of computers, language data processing, neural models, solid-state devices and circuits, etc.

Detailed summaries of papers (three copies) should be submitted by December 15, 1960, to the program chairman,

C. T. Leondes
Department of Engineering
University of California
Los Angeles 24, Calif.

Final papers will be due on March 15, 1961.

INTERNATIONAL CONFERENCE ON MACHINE TRANSLATION OF LANGUAGES AND APPLIED LANGUAGE ANALYSIS

The Autonomics Division of the National Physical Laboratory announces the convening of an international conference on Machine Translation of Languages and Applied Language Analysis, to be held September 5–8, 1961, at the Laboratory, Teddington, Middlesex, England.

Written contributions to the conference are invited from workers engaged directly in research into the machine translation of natural languages and also from those who are concerned with the syntactic or semantic analyses of languages, where such analysis may be of help in achieving machine translation.

Papers should be sent to the Chairman of the papers subcommittee of the appropriate area, depending on the country of origin of authors, to be received by him by January 31, 1961.

USSR, Eastern Europe	To be arranged
USA	Professor L. Dostert Georgetown University 1715 Massachusetts Avenue Washington 6, D. C., U.S.A.
All other countries	Dr. A. M. Uttley, Superintendent Autonomics Div. National Physical Lab. Teddington, Middlesex England

Six copies with six abstracts of each paper should be sent and should be typewritten with double-spacing, on one side of quarto sheets, and must be in one of the official languages of the Conference, *viz.*, English, Russian or French. In the texts of papers, only Roman and Cyrillic characters and strandard-font symbols should be used, any other characters being put into tables and referred to from text. Illustration should be by line drawing only, on separate sheets and using India ink.

The Conference will take place in the new NPL Conference Center, which has a main hall to seat 400 with provision for relay of simultaneous translations of proceedings. These are two smaller conference rooms and ample restaurant facilities. Details of the Conference program and of arrangements for registration of delegates will be announced in the Spring of 1961. The Autonomics Division will be pleased to accept requests for these details at any time.

PUBLICATIONS AVAILABLE

PAPERS ON DATA TRANSMISSION

A collection of current data transmission papers has been issued by the American Institute of Electrical Engineers as Special Publication T-123. These papers were discussed by panels of experts on Monday, October 10, 1960, at the National Electronics Conference in a full-day session devoted to all aspects of this field. The collection includes tutorial papers on coding theory and signal design as well as descriptions and test results on a number of high-speed data transmission systems in the United States and continental Europe, impulse noise measurements on telephone circuits, mathematical models for data errors, and applications of coding to feedback communications and card transmission.

Special Publication T-123 may be ordered by remitting $3.00 to

R. S. Gardner
Editorial Department
American Institute of Electrical Engineers
33 West Thirty-ninth Street
New York 18, New York

The session at NEC was cosponsored by the Communication Theory Committee and Data Transmission Committee of the AIEE and the IRE Professional Groups on Communication Systems and Information Theory.

GOVERNMENT PUBLICATIONS AVAILABLE

Recent (free) government publications of interest to computer people include:

1) "Documentation, Indexing, and Retrieval of Scientific Information, a Study of Federal and Non-Federal Science Information Processing and Retrieval Information Programs," Comm. on Govt. Operations, U. S. Senate; 86th Congress, 2nd Session, Senate Document No. 113; U. S. Govt. Printing Office, Washington, 1960. (283 +xiii pp)

Brief reviews are given of most research efforts in the field, in many cases prepared by the participating organizations.

2) "Use of Electronic Data-Processing Equipment, Hearing before the Subcomm. on Census and Govt. Statistics of the Comm. on Post Office & Civil Service, House of Representatives," 86th Congress, 1st Session, June 5, 1959; U. S. Govt. Printing Office, Washington, 1960. (142 pp.)

The hearing provided representatives of the General Accounting Office and Bureau of the Budget an opportunity to testify regarding the trend of development and use of electronic data-processing equipment in the Federal Government. Status as of December, 1957, is reported in detail. The effect of the adoption and use of electronic data processing systems on personnel utilization and practices is also considered.

This *Notices* Section is open to all who have an announcement of a conference, symposium, session, publication, or other artifact of interest to the PGEC membership. Please send announcements to the *Editor*, who will put them in the first available issue. The right is reserved to edit the announcements, and to decide whether they indeed are aimed at our audience.

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IRE TRANSACTIONS

ON

ELECTRONIC COMPUTERS

Volume EC-9, 1960

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INFORMATION FOR AUTHORS

IRE TRANSACTIONS ON ELECTRONIC COMPUTERS is published quarterly, in March, June, September, and December, with a distribution of over 9000 copies, largely to engineers, logicians, and supervisors in the computer field. Its scope includes the design, theory, and practice of electronic computers and data-processing machines, digital and analog, and parts of certain related disciplines such as switching theory and pulse circuits.

If a paper of widespread interest beyond the computer field is submitted, it will be recommended to the Editor of PROCEEDINGS OF THE IRE for publication. If our reviewers feel that a paper should be submitted to a different IRE TRANSACTIONS, we will so recommend to the author.

Publication time in IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, from receipt of the original manuscript to mailing of the issue, is normally in excess of 5 months, but can be made as little as $3\frac{1}{2}$ months if the occasion demands and the manuscript is carefully prepared.

To avoid delay, please be guided by the following suggestions:

A. Process for Submission of a Technical Paper

1) Send to the Editor three copies of your manuscript, each copy complete with illustrations. (For Letters to the Editor, two copies will do.)

2) Enclose originals for the illustrations, in the style described below. Alternatively, be ready to send the originals immediately upon acceptance of the paper.

3) Enclose a separate sheet giving your preferred address for correspondence and return of proofs.

4) Enclose a technical biography and photograph of each author, or be ready to supply these upon acceptance of the paper. For biography style, see any IRE journal.

5) If the manuscript has been presented, published, or submitted for publication elsewhere, please so inform the Editor. Our primary objective is to publish technical material not available elsewhere, but on occasion we publish papers of unusual merit that have appeared or will appear before other audiences.

B. Style for Manuscript

1) Typewrite, double or $1\frac{1}{2}$ space; use one side of sheet only. (Good office-duplicated copies are acceptable.)

2) Provide an informative 100- to 250-word summary (abstract) at the head of the manuscript. It will appear with the paper and also separately in PROCEEDINGS OF THE IRE.

3) Provide a separate double-spaced sheet listing all footnotes, beginning with "*Received by the PGEC _____," and "†(Affiliation of author)," and continuing with numbered references. Acknowledgment of financial support is often placed at the end of the asterisk footnote.

4) References may appear as numbered footnotes, or in a separate bibliography at the end of the paper, with items referred to by numerals in square brackets, *e.g.*, [12]. In either case, references should be complete, and in IRE style.

Style for papers: Author (with initials first), title, journal title, volume number, inclusive page numbers; month, year.

Style for books: Author, title, publisher, location, year; page or chapter numbers (if desired).

See this or previous issues for further examples.

5) Provide a separate sheet listing all figure captions, in proper style for the typesetter, *e.g.*: "Fig. 1—Example of a disjoint and distraught manifold."

C. Style for Illustrations

1) Originals for illustrations should be sharp, noise-free, and of good contrast. We regret that we cannot provide drafting or art service.

2) Line drawings should be in India ink on drafting cloth, paper, or board. Use $8\frac{1}{2} \times 11$ inch size sheets if possible, to simplify handling of the manuscript.

3) On graphs, show only the coordinate axes, or at most the major grid lines, to avoid a dense, hard-to-read result.

4) All lettering should be large enough to permit legible reduction of the figure to column width, perhaps as much as 4:1.

5) Photographs should be glossy prints, of good contrast and gradation, and any reasonable size.

6) Number each original on the back, or at the bottom of the front.

7) Note item B-5 above. Captions lettered on figures will be blocked out in reproduction, in favor of typeset captions.

Mail all manuscripts to:

Dr. Howard E. Tompkins, *Editor*
IRE TRANSACTIONS ON ELECTRONIC COMPUTERS
Electrical Engineering Department
University of New Mexico
Albuquerque, N. Mex.

Affiliate Status

Members of the professional societies listed below, who are not IRE members, may become AFFILIATES of the PGEC (Professional Group on Electronic Computers), and thus receive IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, by payment of $8.50 annually. Apply to IRE Headquarters, 1 East 79th St., New York 21, N. Y.

(IRE members who join PGEC are currently assessed $4.00 per year.)

Professional Societies Approved for Affiliates to PGEC

American Institute of Electrical Engineers
American Management Society
American Mathematical Society
American Physical Society
American Society of Mechanical Engineers
Association for Computing Machinery
Institute of the Aeronautical Sciences
Institution of Electrical Engineers (London)
Instrument Society of America
Mathematical Association of America
National Association of Accountants
National Machine Accountants Association
Operations Research Society of America
Society for Industrial and Applied Mathematics
Society of Automotive Engineers

IRE TRANSACTIONS ON ELECTRONIC COMPUTERS

Volume EC-9 December, 1960 Number 4

Reviews of Books and Papers in the Computer Field

(See front cover for main contents of issue)